NOTES:

APR-87/ V2A - 2100_H → $3FFF_H$
AX25 - 4000_H → $5B2A_H$

V2A commands

CO - connect
DJ - disconnect
MO - monitor
IN - initialize
CA - callsign
TR - transparent (not implemented)
AB - abort JMP -00
PA - display parameter
M7 - mask to 7 bits
M8 - mask to 8 bits
MM - monitor mode
SE - set parameter
PT - display transparent parameter
HE - HELP

Oxford®
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ESSELTE
10%

README FILE

This diskette contains several files which must be loaded into the VADCG TNC+ to operate. This diskette contains the following files:

```
V2.HEX      - the V-2 link level protocol
V3.HEX      - the V-3 link level protocol
AX25.HEX    - the AX.25 link level protocol
DEFAULTS.HEX - default X.3 parameters and call sign
STOIC2.HEX  - part of STOIC operating system
STOIC.HEX   - main part of STOIC operating system
BOOT.HEX    - bootstrap firmware burned into EPROM at 0
STOICBAS.STC - basic words for STOIC
TIP/LIP.DOC     - documentation for AX.25 program
TIPMOS.DOC      - more documentation for AX.25 program
```

Note that not all combinations of these programs can be present in the TNC+ at one time. This is because some of the addresses overlap. Sorry about that. Future diskettes will contain better coordinated addressing to allow more programs to be resident.

PROCEDURE FOR LOADING 'HEX' FILES

1. Display the 'HEX' file you are about to Load into the TNC+ and determine the address of the first byte to be loaded and the last byte to be loaded. You must look at the first line in the hex file and the second to last line in the file to determine these addresses.

2. Enter the monitor program in the TNC+ and execute the Load command. The command will prompt you for the name of the 'HEX' file you are loading. The name must be a maximum of 8 characters long and does not have to be the same as the name of the file on the diskette. The command will then prompt you for the start and end addresses of the program you are about to load. Enter the addresses determined in step 1.

3. After entering the information required by the command, the command will say it is waiting for the hex file. At this time you must send the 'hex' file to the TNC+ at the same Baud rate that you were using when you issued the command. It is up to the user to provide a program which will do this but I have included an assembly program called PIPMODX.ASM which is a modification to the PIP.COM program available on all CP/M systems. It is the one I use to send the hex files to the TNC+. It will have to be modified for each environment and is only included as an example of the type of program you may need. After installing it on my PIP program I type the following for example:

```
PIP OUT:=V2.HEX   which sends V2.HEX to the serial port.
```

If something goes wrong while the Load command is waiting for the hex file you usually can recover by entering the following line in order to get back into the monitor.

```
:0000000000
```

This simulates the end-of-file to the Load program.

STOIC

STOIC is an operating system and assembler package which runs in the TNC+. Most information about this system can be found on Volume 23 of the CP/M user's group library. STOIC is different

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TIPMOS.DOC - more documentation for AX.25 program

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PIP OUT:=V2.HEX which sends V2.HEX to the serial port.

It something goes wrong while the load command is waiting for the hex file you usually can recover by entering the following line in order to get back into the monitor.

:00000000

This simulates the end-of-file to the load program.

STOIC

STOIC is an operating system and assembler package which runs in the TNC+. More information about this system can be found on Volume 22 of the CP/M user's group library. STOIC is different

from most operating systems but it is very flexible and efficient. However, it is necessary to learn about the system before it can be used. You will need to study the documentation before you can make use of the system.

To get STOIC operational, first load the two HEX files, STOIC and STOIC2. After these have been loaded, execute the STOIC program using the monitor "Program" command. You should get a prompt of, ">0 " on the terminal. At this point you can load the basic STOIC words by sending the file STOICBAS.STC to the TNC. After the basic words are loaded, STOIC becomes smarter.

V-3

Load the two files V3.HEX and DEFAULTS.HEX before executing V-3. Note that V-3 is a new protocol supporting multiple links. Unfortunately, the documentation on how to use the program still is not available.

V-2

Load the single file V2.HEX. This program supports the X.3 and X.28 protocols and full documentation for the protocol and its use is available. It is quite reliable.

AX.25

Load the single file AX25.HEX. The documentation for this program is in the files TIPMOS.DOC and TIP/LIP.DOC. This code is a 'kludge' of Doug Lockhart's original V-1 software but has been altered by a number of different programmers. A better version of AX.25 is being worked on.

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before it can be used. You will need to study the documentation
before you can make use of the system.

To get STOIC operational, first load the two HEX files, STOIC and
STOICC. After these have been loaded, execute the STOIC program
using the monitor "Program" command. You should get a prompt of.
"*D " on the terminal. At this point you can load the basic
STOIC words by sending the file STOICBAS.STC to the TNC. After
the basic words are loaded, STOIC becomes smarter.

V-C

Load the two files VC.HEX and DEFAULTS.HEX before executing V-C.
Note that V-C is a new protocol supporting multiple links.
Unfortunately, the documentation on how to use the program still
is not available.

V-C

Load the single file VC.HEX. This program supports the X.C and
X.CE protocols and full documentation for the protocol and its
use is available. It is quite reliable.

AX.CC

Load the single file AXCC.HEX. The documentation for this
program is in the files TIPMOD.DOC and TIPVLIP.DOC. This code is
a 'kludge' of Doug Lockhart's original V-1 software but has been
altered by a number of different programmers. A better version
of AX.CC is going worked on.

INITIALIZATION

In order to use the TNC+ for the first time using the firmware provided in the firmware EPROM some special steps must be taken as follows.

When the TNC+ is turned on for the first time after construction the RAM memory contains random data. The RAM memory can contain random or incorrect data after certain types of software or hardware failures as well. Since some of the information in RAM is normally used to control certain initialization features, the TNC+ may not be initialized correctly upon power on or reset. The first step in bringing up a newly built TNC+ is to modify certain memory addresses so that initialization will work correctly.

When powered on for the first time you may not get any response from the TNC+ or garbage messages may appear on the terminal. Do not be alarmed - this is a normal situation. Perform the following procedure to set up the TNC+.

1. Set jumper positions for memory configuration A as described on Page 27 of the Assembly instructions. Do not have any memory write protected.

2. Connect your terminal to the TNC.

3. Power on the TNC+.

4. Give the TNC a Trap interrupt by pressing the trap pushbutton if you have installed one, or otherwise by shorting the centre pin of the Trap switch connector (J11) alternately to the outer two pins of the Trap switch connector.

5. Do an Autobaud operation by alternately typing '.' and ',' (period and comma) on the terminal keyboard. After a few key depressions the TNC+ will print some information on the terminal and prompt you for a monitor command.

6. Display the directory using the Dump command. It is located at addresses 2000 to 20FF hexadecimal. Note that all memory addresses are in hexadecimal. The directory will undoubtedly contain random data. Using the Store command, store 0 at the following locations in RAM if they are not already 0. (Note that you should not have the memory write protected at this time.)
2000, 2010, 2020, 2030, 2040, 2050, 2060, 2070, 2080, 2090, 20A0, 20B0, 20C0, 20D0, 20E0 and 20rol-C. This procedure indicates to the firmware that all 16 directory entries are unused.

7. Use the Store command to enter your call sign at address FFF8 to FFFE in memory. Use the hexadecimal representation of the upper case Ascii characters. There is no command to do this but it usually only has to be done once.

8. Use the Store command to set memory address FF88 to control AutoBaud and automatic program entry as follows

Bit 0 = 0 use autoBaud when TNC is reset
Bit 0 = 1 use speed and format from last autoBaud when the TNC is reset.
Bit 1 = 0 enter monitor after system reset

Bit 1 = 1 automatic program entry after reset (put program address at FF86)

Bits 2 through 7 are not used

I suggest setting FF88 to 1 initially.

Note that when autoBaud is done after reset it will start echoing all the characters typed on the keyboard. At this point you have to enter a number from 0 to 2 to continue. This number represents the type of flow control you wish to use but is not otherwise used at present.

Also note that when using the firmware monitor interrupts are disabled and the output character rate is deliberately slowed down so that flow control will be unnecessary even with very slow terminals.

After this procedure, you should automatically come up at the desired Baud rate and format of your terminal when the TNC+ is powered on or reset and your callsign should be displayed by the firmware monitor.

You may now proceed to load programs and protocols into the TNC.

AX.25

Sep. 15, 1985

TIP

The LIPM05 version of LIP/LIPM has been modified to utilize the new national packet HDLC Standard for Link Level protocol. Key features of this new protocol are call sign addressing, an optional repeater field, asynchronous balanced mode of operation, the definition of a protocol ID field, a longer maximum packet length, and changes in the meaning and use of the control field to adhere to the usage prescribed by the new standard. Some new user commands have been added along with a useful debugging command.

The M04 version of LIPM/TIPM was the first attempt at call sign addressing. This edition is now obsolete and users should move to Revision 5.

The M03 version of TIP has been modified to make it completely transparent to the characters being sent through it. Most of the commands to the TIP program were changed from single control characters (which could never be transmitted through the LIP) to "escape sequences". These are sequences started by ONE particular SPECIAL character (currently set to escape [ESC], ASCII code 1B hex) and followed by one or two graphic (printing) characters. The SPECIAL character is purposely chosen to be one not normally used by most programs, so as to not "get in the way" in most situations. In this way, any characters, even 8-bit binary characters, can be sent through the TIP. A single SPECIAL character can be sent out by sending two in succession to the TIP program. Some control characters are still optionally recognized as editing and flow-control characters in the default configuration, but this can be disabled by keyboard commands if desired.

Following is a list of the current commands (the symbol [ESC] indicates escape):

"[ESC][ESC]	send a single [ESC] as a normal character
[ESC]C	Connect (ex. KA6M[ESC]C or KA6M 1[ESC]C)
[ESC]D	Disconnect (old ^Y)
[ESC]E	Echo enable
[ESC]NE	No Echo
[ESC]I	Initialize the TIP program (almost like a hardware RESET)
[ESC]L	automatic LF after CR
[ESC]P	force Packet to be sent
[ESC]R	set Repeater Address Field (ex. KA6M 2[ESC]R)
[ESC]NR	set No Repeater Address condition
[ESC]S	recognize Special (control) characters
[ESC]T	set packet type (control field) (ex. 00[ESC]T defaults ctl to 00H
[ESC]NS	do Not recognize Special characters
[ESC]O	set 0th byte of info field, the protocol ID byte, to new default
[ESC]7	mask data to 7 bits
[ESC]8	mask data to 8 bits

The alphabetic characters following [ESC] can be in either lower or upper case. The default settings after a hardware or software reset are as follows:

[ESC]E	Echo on
[ESC]NL	No automatic LF after CR
[ESC]NR	No Repeater address range
[ESC]S	recognize Special control characters
[ESC]7	mask data to 7 bits

The bell is sounded if an unrecognized character is seen following the [ESC], and the character is ignored. Both BACKSPACE and DELETE are recognized as character editing commands (when [ESC]S is on), and they echo BS-SPACE-BS to erase the last character, except when at the first column, when a bell is echoed, as before. No checks are made for non-printing characters, so the erasure may not be perfect. The SPECIAL character can be changed by editing one EQU statement, and '_' can be echoed for DELETE instead of BS-SPACE-BS by changing another EQU statement. The Initialize (reset) command just jumps to location 0 without activating the external hardware RESET line, so it may not be completely equivalent to a hardware RESET function.

When the [ESC]S option is on (recognize Special control characters), CR causes a packet to be sent. Also, [ESC]P ALWAYS sends the existing packet, even if it is only one character. When the [ESC]NS option is in effect, the CR does NOT cause the packet to be sent, just the [ESC]P.

The following control characters are recognized when the [ESC]E option is on:

Linefeed	- Place linefeed in the buffer, echo it, no other special actions.
Car. Ret.	- Place CR into buffer, echo it, and send the packet.
Control D	- Debug Dump (ex. 10^D dumps 256 bytes at1000H)
Control E	- Clear the screen
Control Q	- Continue output to the attached terminal or computer.
Control S	- Suspend output to the attached terminal or computer.
Control U	- Cancel the current input line and echo CR-LF.
Escape	- Place into buffer and echo as '$'.
Delete	- Erase a character and echo BS-SPACE-BS or '_', depending on assembly option. Echo a bell if at start of line.
Backspace	- Erase a character and echo BS-SPACE-BS. Echo a bell if at start of line.
Others	- Place character into the buffer and echo to the terminal.

When the [ESC]NS option is in effect, the above control characters are treated as ordinary characters and cause no special action. In this mode, the ONLY special character is the [ESC] (or other equivalent character, if this was changed before reassembling the TIP).

Currently there are only three conditions which will cause a packet to be sent (from a non-host station). A CR will send the packet if the [ESC]S option is on, and a [ESC]P will always send the packet. In addition, if the input exceeds MAX characters, the

current input will be sent.

The repeater will repeat packets if its address is found in the optional address field. The [ESC]R command may be used to set the contents of this field. The [ESC]NR command will remove the optional repeater address from each packet.

The code associated with "connection" was also changed. It is now possible to type the target callsign in lower case, and without trailing blanks. The program automatically converts the target callsign to upper case and adds trailing blanks if the call is shorter than 6 characters. This is currently done in the TIP (so that it was not necessary to change the LIP as well). If a seventh character is typed it will be used as the call's SSID. You will see *CNCT** when a connection is made. A *DISC** will appear when the connection is broken.

The flow control logic was changed to include the RTS and CTS signals from the 8250 as well as the ^S and ^Q characters (if the [ESC]S option is on). When CTS is false (low EIA level), serial transmission of characters to the terminal is inhibited. NOTE THAT THIS MAY REQUIRE A SLIGHT MODIFICATION TO THE TIP HARDWARE IN ORDER TO GET ANY CHARACTERS PRINTED OUT FROM THE LIP. The CTS line for the terminal port (at the EIA interface) must be HIGH for normal operation. It is recommended that this line be tied to +5 or +12 volts through a 5K to 15K resistor, so that an external signal can override the high level and stop transmission if desired. Also, RTS (an output from the 8250) is normally high. When the terminal input buffer becomes full, this line now goes low at the same time as the ^S is sent to the data source. If the [ESC]NS (No Special characters) option is active, the TIP neither sends or recognizes ^S and ^Q for flow control; ONLY the RTS and CTS lines are used, so as to make the program completely transparent to the characters which are being sent.

Known bugs at this time include these glitches:

1. If the input line is connected to a host computer, and the async line is run at high speed, character overrun (loss) can occur. So much interrupt time processing and checking has been added that the work involved, particularly at end-of-packet time, is more than can be done before the the next character comes in. Typically 1-2 characters can be lost if the input is used at 9600. Try running the input line at slower speeds under these conditions. Some rework of the code is required to remove all that character-by-character processing from inside the interrupt system. It impacts the link, too, as an SDLC data underrun is now possible.

2. In monitor mode there is still no interlock during a buffer overrun.

3. The proper use of the P/F bit and correct methods for recovering from timeouts and receiver-not-ready conditions is still being debated by the protocol designers. The VADCG and TAPR implementations differ in this regard. The VADCG code has to be carefully reviewed for its adherence to the protocol specs. The current release probably has some violations which will be fixed in 5.2 or later releases. Sometimes, if the TAPR send a RNR to the VADCG, there is not a successful restart. This could

occur if the receiving station has a slow output or has held Ctl-S for a long time.

June 19, 1984

This document describes the changes made to the TIP and LIP modules of the VADCG board AX.25 software which produced LIPM 5.1A and TIPM 5.2A. Major modifications were made to allow multiple repeater addresses, improved end-of-line (carriage-return/line-feed) handling and a new host mode option.

The following commands have been altered:

[ESC]R
[ESC]NR

The [ESC]R command (set repeater address) has been changed to allow the specification of up to eight repeater addresses in the address field of the AX.25 frame. Syntax for this command is now:

RRRRRRSRRRRRRS.....RRRRRR[S][ESC]R

Each repeater address except the last in the string of addresses MUST be seven characters in length. The first six characters are the repeater call sign, the last is the SSID. If the call sign is fewer than six characters in length, it must be blank filled. The last address need not have blanks or an SSID following it if the SSID is 0. Examples:

K1FFK 0W1AW 5[ESC]R (frame is repeated by K1FFK-0, then W1AW-5)
W1AW 5K1FFK[ESC]R (frame is repeated by W1AW-5, then K1FFK-0)

The [ESC]NR command turns off the repeater addressing.

Whenever the repeater address is changed, the retransmission timer value (T1 of the AX.25 protocol) is set to a calculated value. The value will naturally increase as the number of repeaters is increased. The shortest value is used when there is no repeater address (about 3 seconds). This timer value may be changed by the [ESC]W command (see below), but it will be set once again to the calculated value if the repeater address is set again.

The repeater address is set by either the [ESC]R command or by connection with another station after receipt of that station's SABM frame.

The following commands have been added to the TIP:

[ESC]A (alter user call sign)
[ESC]B (display baud rate menu)
[ESC]G (goto machine level monitor)
[ESC]H (turn host mode on)
BREAK (exit from HOST mode)
[ESC]K (change relay delay time)
[ESC]W (set T1 wait timer)
[ESC]X (optional extended ROM jump)

The host mode, which was formerly an assembly option, is now

available via keyboard command. When [ESC]H is in effect, characters received from the host will not be echoed. In addition, the determination of the end of an outgoing frame is no longer by characters. Instead, a timer is used. As each character is received from the host, the timer is reset. If the timer runs out before another character is received, the characters in the input buffer will be transmitted as a frame. This operation enhances the use of a host computer which issues prompts terminated by a variety of different characters. (Note: CR is still a frame terminator unless the [ESC]NS command is invoked.) Invocation of the [ESC]H command performs an assumed 00[ESC]L command as well. Note: no monitor mode exists in host mode. The exit from Host mode is by sending a BREAK character to the TNC.

The [ESC]W command is used to alter the value of the T1 timer. The syntax of this command is as follows:

HH[ESC]W

where HH represents two hex digits. The timer can be set to any value from 00 to FF. Since the timer consists of a 16 bit counter, these digits are used to set the most significant 8 bits of the counter. The least significant bits are always set to FF, which avoids the possibility of a 0 timer value.

The [ESC]X command, which may be included as a TIP assembly option, is used to jump to a ROM located at 1000H. This can only be useful on a board which has been modified to increase the ROM address space. If this is used, the interrupts from the 8273 and 8250 will be vectored to that ROM space. See the program listing for further info.

In order to provide an indication of connection status to a host computer, the terminal port DTR line is now set to a TRUE (high) state when a connection is made and returned to a FALSE (low) condition when the connection is terminated. This line may be used to reset the host computer if desired. On a CP/M machine, the BIOS may be modified to warm-boot the system when a transition from the low state to the high is detected.

The only know bug in this software has to do with the RTS/CTS handshaking on the terminal port. Occasionally, the TNC fails to return the CTS line to a true state when the buffers empty. This "hang-up" seems to correct itself when a disconnect occurs.

Any questions regarding these modifications to the software should be directed to:

Howard Cunningham
AMRAD
P. O. Box 6148
McLean, VA 22106-6148

VOL 7 DOC

June 7, 1986

This Volume 7 diskette is an updated version of the original "HEX" diskette in Volume 1. It contains the following changes and improvements:

1. The AX.25 protocol has many bugs fixed and is much easier to use than the version on Volume 1. It supports the AutoBaud function in the BOOT eprom and uses the ESC key to enter commands to make it more like the V-2 implementation.

2. The BOOT.COM file now has a working memory file capture program operational using the "C" command. This now allows a newly built TNC+ without any protocols or 'smarts' to be uploaded from another TNC+. The (C)apture program works with the memory file transfer program which is now provided with the V-3 protocol. See the V-3 protocol below for more information.

3. The V-3 protocol provided on this diskette is still in the experimental stages. This version has a number of fixes not contained in the previous version on Volume 1. However, most importantly, it now has a working memory file transfer program which can be used to send a memory file or protocol to another TNC+. Although the user's manual for this implementation has still not been written, the following description should be enough to allow the use of this important facility.

The command structure of V-3 is in general similar to the V-2 implementation. The following command will send a memory file to a TNC+ using the boot command, '(C)apture':

SF <filename> <callsign>

for example:

SF AX25 VE7ABC

will send the memory file AX25 to node VE7ABC.
Note that each command should be followed by a carriage return and also note that VE7ABC must have issued the 'C' command for the transfer to work. Also, the transfer requires operator intervention at VE7ABC as the operator is asked whether he wishes to accept the transferred file.

4. The V-3 protocol has not been changed substantially since the previous release in Volume 1. Parameter 38 now controls whether bringing DTR from active to inactive will force a disconnect. If parameter 38 is 0, a change in DTR level will have no effect. If parameter 38 is 1, a transition of DTR to inactive will force a disconnect.

5. The STOIC system has not been changed from the previous release in Volume 1.

This diskette contains source code for the V-2 protocol for the VADCG TNC+. To assemble the source code you will need the Digital Research RMAC (c) assembler and to link the modules you will need the Digital Research LINK program. These programs are not provided on the diskette. (I have been told that the Microsoft (c) M80 assembler and L80 linker are very similar and the programs may be modified slightly to work with the Microsoft programs which are generally more available than the Digital Research programs. I have not tried to use the Microsoft programs but would appreciate any feedback from anyone using these programs to assemble and/or link the programs on this diskette.)

The sequence of commands to generate a V2.HEX file which can be loaded into the TNC+ at location 2100H is as follows:

```
RMAC LIP2
RMAC TIP2
RMAC NIP2
LINK V2=MASTER3.LIP3,LIP2,NIP2,TIP2[L2100]
UNLOAD V2 2100
```

To create a V2.HEX file to be loaded at a different address, substitute the desired hexadecimal address for the '2100' appearing twice in the above command sequence.

END (SOURCE DISK)

Oxford®
NO. 733 1/3
ESSELTE
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VANCOUVER AMATEUR DIGITAL COMMUNICATIONS GROUP

Preliminary

ASSEMBLY INSTRUCTIONS

for the

VADCG TNC +

Terminal Node Controller

May 4, 1986

POLICY

The Vancouver Amateur Digital Communications Group is a non-profit organization. This TNC board was developed by members of the VADCG - the group that developed the first TNC. The VADCG does not have sufficient volunteers to do the work of supplying the boards, parts kits, documentation and software for the TNC + and so the job is being done by one of the developers of the board on a royalty basis. The VADCG is relying on voluntary donations to continue their work in raising the technical level of Amateur Digital Communications. If you wish to assist the VADCG financially please send contributions to the following address:

V.A.D.C.G.
9531 Odlin Road,
Richmond, B.C. V6X 1E1

Orders for the TNC + board, parts, software, etc. should be sent to:
Lockhart Technology
9531 Odlin Road,
Richmond, B.C. V6X 1E1

DISCLAIMER

In supplying this printed circuit board, neither the Vancouver Amateur Digital Communications Group nor Lockhart Technology makes any representations or warranties as to its usefulness in any particular application. There is no committment to supply parts for the board, software for it, or service for it. Availability and price are subject to change without notice.

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Lockhart Technology
9531 Odlin Road
Richmond, B.C. V6X 1E1 Canada
(604) 278-5601

VADCG TNC+ PARTS LIST - GROUP 1

(Required for upgrade from original VADCG TNC)

INTEGRATED CIRCUITS

QTY	DESCRIPTION	CKT. SYMBOLS
1	7406 Hex inverter	U9
1	4040 CMOS binary divider	U12
1	ICL8212CPA voltage comparator	U17
1	2764 8K by 8 EPROM	U18
7	6264 MOS 8K by 8 RAM	U19-U25

RESISTORS

1	1000 ohm 10-pin SIP	R1
3	10k ohm, 1/4 watt, 5%	R2,R8,R27
7	270 ohm, 1/4 watt, 5%	R3-R7,R13,R14
2	2200 ohm, 1/4 watt, 5%	R9,R10
2	4700 ohm, 1/4 watt, 5%	R11,R12
1	33k ohm, 1/4 watt, 5%	R15
1	32.4k ohm, 1/4 watt, 1%	R16
1	1.5m ohm, 1/4 watt, 5%	R18
1	100k ohm, 1/4 watt, 1%	R19
1	360 ohm, 1/4 watt, 5%	R20
2	4.7k ohm, 10-pin SIP	R21,R22

DIODES

4	LED, red	CR1,CR2,CR3,CR4
5	1N4148, silicon	CR5,CR6,CR7,CR8,CR9

TRANSISTORS

2	PN3645	Q1,Q2

CAPACITORS

10	330 pF, 500 volt, Ceramic	C1-C6,C8-C11
12	.1 uF, 100 volt, Monolithic	C7,C12,C13,C15,C16,C19,C20, C21,C25,C27,C28,C31
1	1 uF, 16 volt, Tantalum	C14
2	20 pF, 100 volt, Ceramic	C17,C18
1	220 uF, 16 volt, Electrolytic	C22
1	470 uF, 6.3V, Electrolytic	C26

CONNECTORS

3	DB25S 25-pin straight	J1,J2,J3
1	16-pin, male DIP header	J4
1	14-pin, DIP socket	J5
1	16-pin, DIP socket	J6
7	2-pin, male header	J7,J12-J17
1	6-pin, male header	J8
1	20-pin, male DIP header	J9
2	3-pin, male header	J10,J11
1	Weco 95GDS 20.871.054	J18

IC SOCKETS

1	8-pin DIP	U17
8	14-pin DIP	U1-U5,U9,U11,U16
3	16-pin DIP	U10,U12,U13
1	20-pin DIP	U15
8	28-pin DIP	U18-U25
4	40-pin DIP	U6,U7,U8,U14

MISCELLANEOUS

1	8PST DIP switch	S1
1	3.6 Volt Lithium battery	B1
1	'Mousetail'	
1	PC board, TNC+, Issue 2, M2	
8	.1 inch push-on jumpers	
1	16-pin, .3 inch male DIP header	
1	14-pin, .3 inch male DIP header	
2	push-on wire jumpers	

VADCG TNC+ PARTS LIST - GROUP 2

(Required if not upgrading from original VADCG TNC)

INTEGRATED CIRCUITS

QTY	DESCRIPTION	CKT. SYMBOLS
2	1488 RS232 transmitter	U1,U5
3	1489 RS232 receiver	U2,U3,U4
1	8273 HDLC/SDLC controller	U6
1	8255 parallel interface	U7
1	8250 UART	U8
2	74LS138 1 of 8 decoder	U10,U13
1	4024 CMOS binary divider	U11
1	8085 microprocessor	U14
1	74LS373 8 bit latch	U15
1	74LS00 quad NAND gate	U16

MISCELLANEOUS

1	4.9152 mHz. crystal, HC-18/U	Y1

VADCG TNC+ PARTS LIST - GROUP 3

(Chassis kit parts)

1	chassis bottom section
1	chassis top section
1	SPDT pushbutton
1	SPST pushbutton
1	2-conductor header connector MTA-100
1	3-conductor header connector MTA-100
1	6-conductor header connector MTA-100
4	LEDs
1	Length of insulated wire
1	rubber grommet
8	6-32 x 3/8" screws
1	stick-on label

VADCG TNC+ PARTS LIST - GROUP 4

(Switching power supply parts)

INTEGRATED CIRCUITS

2	TL497 switching regulator	U26,U27

RESISTORS

1	1200 ohm, 1/4 watt, 5%	R23
1	11k ohm, 1/4 watt, 5%	R24
1	1 ohm, 1/4 watt, 5%	R25
1	10k ohm, 1/4 watt, 5%	R26
1	.1 ohm, 2 watt,	R28
1	100 ohm, 1/4 watt, 5%	R29
1	47 ohm, 1/4 watt, 5%	R30
1	3920 ohm, 1/4 watt, 1%	R31
1	1210 ohm, 1/4 watt, 1%	R32

DIODES

2	MR854	CR10,CR11
1	1N4003	CR12

CAPACITORS

2	.1 uF, 100 volt, Monolithic	C23,C33
2	150 pF, 100 volt, Mylar	C24,C30
1	39 pF, 100 volt, Ceramic	C29
1	220 uF, 25 volt, Electrolytic	C32

TRANSISTORS

1	2N6126	Q3

MISCELLANEOUS

1	Heat sink	
2	Toroid cores	L1,L2
1	Length of #18 double enameled wire	
1	Length of #22 double enameled wire	
2	'Mousetails'	
2	Terminal pins (large)	
2	Terminal pins (small)	

IC SOCKETS

2	14-pin DIP sockets	U26,U27

VADCG TNC+ SPECIFICATIONS

HARDWARE

Timing
The 8085A Microprocessor uses a 4.9152 MHz. crystal to provide a master system clock of 2.4576 MHz. A binary dividing chain provides frequencies from 307.2 kHz. down to 4.6875 Hz. for HDLC controller data rates and software clocking. The timing chain may also be used for interrupting the microprocessor at selected intervals.

Memory
The full 64k addressing space is supported and the following combinations of RAM/EPROM are supported by jumper selection:

8k EPROM - 56k RAM
16k EPROM - 48k RAM
32k EPROM - 32k RAM

The RAM below 8000 (Hexadecimal) in the address space may be selectively write protected by jumper selection. All RAM is backed up by a Lithium battery expected to last about 5 years if the TNC+ is powered off. If the TNC is powered on, it should last for the shelf life of the battery which is greater than 10 years. 8 sockets for 2764 type EPROMs and 6264LP RAM chips are provided. A Voltage comparator automatically disables memory and resets the microprocessor when the supply voltage drops into an out of specification range. This prevents the microprocessor from writing garbage data into random memory locations during power brown-outs.

Serial Port
Uses an 8250 UART with internal Baud rate generator using industry standard 1488 and 1489 RS-232 drivers to a standard female DB-25S connector. The connector may be configured as either a DCE or DTE (or non-standard connections) with a jumper plug provided. The RS-232 signals supported are:

Transmit Data	TD	*
Received Data	RD	*
Request to Send	RTS	
Clear to Send	CTS	*
Data Set Ready	DSR	*
Carrier Detect	CD	*
Data Terminal Ready	DTR	
Ring Indicator	RI	

The serial port can be used in polled mode or interrupt driven mode by the software. Changes in status of the lines marked with an '*' can generate interrupts. The serial Baud rate, data format, stop bits, etc. are under complete software control allowing for automatic selection of data speed and format (Autobaud). Standard Baud rates supported are: 38,400, 19,200, 9600, 4800, 2400, 1200, 600, 400, 300, 150, 134.5, 110, 75, 45.45. Many other non-standard speeds are also supported by the hardware.

Modem port
An Intel 8273 HDLC/SDLC protocol controller chip is used with 1488 and 1489 RS-232 drivers and an industry standard DB-25S (female) connector supporting the following signals:

Transmit Data	TD	*
Received Data	RD	
Request to Send	RTS	*
Clear to Send	CTS	
Data Set Ready	DSR	
Carrier Detect	CD	
Transmit Clock	TC	
Receive Clock	RC	
Data Terminal Ready	DTR	*
Signal Quality	SQ	
Ring Indicator	RI	
Data Speed Select	DSS	*

The output signals are indicated by an '*'. In addition, +12 and -12 voltages are supplied on pins 9 and 10 of the DB-25S connector to supply power to the modem. The on-board switching power supply has excess capacity to power a modem. A separate header connector provides the above signals at TTL levels along with +5, +12 and -12 voltage levels for an internal modem (inside the same cabinet). Both full duplex and half duplex, synchronous and asynchronous modems are supported by means of on-board jumpers. Asynchronous modem speeds at the following Baud rates are supported by means of on board jumpers: 9600, 4800, 2400, 1200, 600, 300, 150, 75. Other asynchronous modem speeds (such as 400 Baud) are possible up to 9600 Baud if clocks are provided on RC and TC by the modem. Synchronous modems are supported at any Baud rate up to 64,000 Baud. (Baud rate is controlled by the modem.) Note that the Baud rate may be limited by the software being used.
The 8273 transmit and receive functions are completely independent allowing for full duplex operation. Separate receive and transmit interrupts are provided allowing for interrupt driven software.

Parallel Port
An 8255A Programmable Parallel Interface provides 24 I/O lines of TTL level signals on a DB-25S connector. These lines may be programmed under software control in several different modes of operation such as input or output, handshaking, bidirectional and interrupt control. They may be programmed to drive a printer with a Centronics parallel interface or provide control lines for specialized equipment. The parallel port may be operated under interrupt control.

Configuration Switches
An 8-position DIP switch is provided which can be read by software.

Indicator LEDs
There are 4 on-board LEDs which can be turned on and off by software. A header is provided for mounting the LEDs off board if desired.

Trap Switch
Circuitry and a connector is provided to allow for an off-board Trap interrupt switch. (Non-maskable interrupt) This is very useful for a software developer to analyse software failures.

Reset Switch
Circuitry and a connector is provided to allow for an off-board Reset switch or pushbutton. A reset function is automatically performed when the TNC+ is powered on.

Power supply
An on board switching power supply and regulation is provided to supply all voltages needed by the board as well as power for off board circuitry such as modems. Nominal DC power of +10 to +15 Volts is required but typical operation is between +7 Volts and +18 Volts. A connector is provided to operate the TNC directly from regulated +5, +12 and -12 Volts without the need of the switching power supply components. When the board is not supplying off-board power the measured current consumption without CMOS components is:

290 mA at 17 Volts
340 mA at 12 Volts
480 mA at 7 Volts

The on board switching power supply supplies regulated power at the following currents for off-board devices.

5 Volts at 2 Amperes
-12 Volts at approximately 120 mA.

The input power Voltage (+10 to +15 Volts) is also available.

PC Board
7.75 X 8.5 inches (197 X 216 mm.) Double-sided G-10 Glass Epoxy with plated through holes. The board is silk-screened and solder masked.

Upgrade
Users with the original VADCG TNC board should note that this board is exactly the same size as the original board with mounting holes and edge connectors in the same position as the original board. The major components from the original board such as the 8273, 8255, 8250, 8085, 1488s, 1489, 4024, 74LS373, 74LS132s, 74LS00 and 4.9152 MHz. crystal can be removed and installed on the new board and the old power supply can be used to power it instead of using the on-board switching power supply components. This will significantly reduce the cost of upgrading to the new board. A special parts kit will be available for those who already have the original VADCG TNC and are upgrading to the TNC+.

Price and availability
The TNC+ PC board, assembly instructions, parts list, and circuit diagram are available now for $38 U.S. or $50 CDN. postpaid. The parts kits will be available near the end of December and cases sometime in January. Parts kits and case prices to be announced.

Make cheque or money order payable in U.S. or Canadian funds to:

Lockhart Technology
9531 Odlin Road,
Richmond, B.C. V6X 1E1
Canada

Sorry, no Visa or MC orders.

DESIGN PHILOSOPHY

It is important to understand the design philosophy behind the VADCG TNC+ as it is not the same as most of the TNCs on the market. Factors which went into the design of this TNC are:

1. We wanted to modernize the TNC while still keeping faith with the purchasers of the original VADCG TNC designed in 1979. We did not want to negate the substantial effort which went into software for the original board or the investment in hardware.

2. We wanted to provide a more 'open' system than most of the other TNC manufacturers. The source for most of the software running on the board is available.

3. We wanted a better way to upgrade and distribute new software for the TNC than by replacement of EPROMs. The large battery backed up RAM space combined with selectable write protected areas allows programs to be distributed in five different ways.

1. Programs may be loaded from a 'HEX' file from a computer.

2. Programs may be loaded from a remote computer using a packet radio link.

3. Programs may be transferred directly from one TNC to another using a packet radio link without the aid of a computer.

4. Programs may be loaded over a telephone connection.

5. Programs can still be provided in burned in EPROMs as has been done in the past.

4. We wanted to provide a system that software developers could use. With this TNC, the software developer does not have to own an EPROM programmer and eraser. New programs can be loaded quickly from a serial port on the development system. In addition, an operating system using a version of FORTH and an assembler is already operating and available which runs on the TNC+ itself. With these tools, a developer can program directly on the TNC in either assembly language or higher level Forth type words. This in fact, allows the TNC to operate as an independent microcomputer development system.

5. We wanted to increase the flexibility and function of the TNC rather than strip it to bare essentials as is being done by others. The parallel port allows use of a printer and terminal simultaneously or provides signals for remote control applications. The serial port supports automatic speed and format selection (Autobaud) over a wide range. The Baud rates are not just the binary rates between 300 and 9600 but go up to 38,400 Baud and down to DC including all standard speeds in this range as well as many non-standard speeds. For example, speeds of 45.45, 110, and 134.5 are supported by the hardware.

Instead of an on-board modem providing only low speeds of 300 or 1200 Baud, the TNC+ has an industry standard connector to an off-board modem and supports synchronous modems at Baud rates up to 64,000 Baud and asynchronous modems up to 9600 Baud and both NRZ and NRZI encoding is supported at all Baud rates. The future of Amateur packet radio urgently requires a move to higher Baud rates. The TNC+ can use almost all existing standard modems such as Bell 202, 212A, 103, etc. as well as many others which have not seen common use in Amateur radio as yet. (An off-board radio modem is available from the VADCG which supports changes from 300 to 1200 Baud with switch selection and requires no tuning up and is powered directly from the TNC+.)

Compare this for example, to the off-board modem connector in the TAPR TNC-2 which does not use a standard connector or standard voltage levels (TTL instead of RS-232), only supports the more expensive synchronous modems and requires special signals which are not supplied by standard modems.

FIRMWARE

The TNC+ parts kit will come with a single programmed 2764 EPROM containing code which will allow bootstrap loading of the battery backed up RAM through the serial port or by a radio link to another TNC+. It contains the Autobaud routines and memory file system as well as drivers for the serial, parallel and HDLC ports. The firmware contains buffer and queue management routines and common routines which can be used by programs in RAM and a monitor program which allows for the displaying of registers and status, the displaying and changing of memory, and the display of the directory of memory files and programs. The firmware allows for all but the Trap and Restart interrupts to be vectored to RAM addresses.

VADCG TNC + Assembly Instructions

SOFTWARE

All I/O port addresses remain the same as in the original TNC board so the many programs written for the original board should still run in the new board. Much time and effort has been made developing these programs and that effort should not have been wasted. Some minor modification of some of these programs may be required due to the expanded address space of the new board.

At the present time, the firmware is operational with all features except for the radio link file transfer. This final feature is being tested and expected to be available when the parts kits become available - in January, 1986.

The Forth-like operating system (STOIC) and integrated 8085 assembler are available now. Additional low level communication words will be available in January.

The V-1, V-2 and AX.25L2 protocols are being integrated at the present and expected to be available sometime in January, 1986.

The V-3 state exchange protocol first release is expected to be available sometime in February, 1986.

Note that the source code for most of these programs will be made available on diskette.

ASSEMBLY INSTRUCTIONS

The following instructions make the assumption that the assembler has soldered PC boards of this type previously. If this is not the case, I recommend that the assembler obtain assistance from someone experienced in soldering small electronic components and electronic kit assembly.

To assemble the TNC+ you will need the following items which are not supplied with the kit:

1. A small-tipped, low powered electric soldering iron of about 25 watts - a soldering iron with controlled tip temperature of 700 deg. F. is preferred.

2. Rosin-core solder of small diameter oabout .04 inch). Either 60/40 or 63/37 is acceptable. Do not use acid-core solder.

3. Small diagonal side-cutters.

4. Small needle-nose pliers.

5. An accurate voltmeter (1% or better preferred)

TNC+ CIRCUIT BOARD ASSEMBLY

( ) Check that all components in Group 1 and Group 2 of the TNC+ parts list are at hand.

( ) Position the TNC+ Issue 2, M2 circuit board on the working surface in front of you so that the silk screen printing is readable.

( ) Inspect all IC sockets for bent pins. Straighten any bent ones carefully before proceeding.

NOTE: When installing the IC sockets in the following steps note that each socket has a notch or bevelled corner at one end. Also note that one end of the silk screen symbol has a notch at one end. Insert the IC so that the notch or bevel on the socket is aligned with the notch on the IC symbol.

NOTE: When soldering IC sockets it is a good idea to initially solder two diagonally opposite pins, then attempt to rock the IC back and forth as a check to see that the socket is seated properly before soldering the remaining pins. If it is found to be poorly seated, it is a simple matter to re-seat the socket by reheating one of the soldered pins while applying pressure on the socket.

NOTE: For good soldered connections, you must keep the soldering iron tip clean. Wipe it often on a damp sponge, or damp cloth or paper.

Install and solder the following IC sockets:

( ) U17 8-pin
( ) U1 14-pin
( ) U2 14-pin
( ) U3 14-pin
( ) U4 14-pin
( ) U5 14-pin
( ) U9 14-pin
( ) U11 14-pin
( ) U16 14-pin
( ) J5 14-pin
( ) U10 16-pin
( ) U12 16-pin
( ) U13 16-pin
( ) J6 16-pin
( ) U15 20-pin
( ) U18 28-pin
( ) U19 28-pin
( ) U20 28-pin
( ) U21 28-pin
( ) U22 28-pin
( ) U23 28-pin
( ) U24 28-pin
( ) U25 28-pin
( ) U6 40-pin
( ) U7 40-pin
( ) U8 40-pin
( ) U14 40-pin

( ) Check for solder bridges and cold solder joints. Re-solder if necessary.

Install the following 1/4 watt, 5% tolerance resistors on the board. Solder and trim the leads.

( ) R2 10k ohm (brown-black-orange-gold)
( ) R3 270 ohm (red-violet-brown-gold)
( ) R4 270 ohm (red-violet-brown-gold)
( ) R5 270 ohm (red-violet-brown-gold)
( ) R6 270 ohm (red-violet-brown-gold)
( ) R7 270 ohm (red-violet-brown-gold)
( ) R8 10k ohm (brown-black-orange-gold)
( ) R9 2200 ohm (red-red-red-gold)
( ) R10 2200 ohm (red-red-red-gold)
( ) R11 4700 ohm (yellow-violet-red-gold)
( ) R12 4700 ohm (yellow-violet-red-gold)
( ) R13 270 ohm (red-violet-brown-gold)
( ) R14 270 ohm (red-violet-brown-gold)
( ) R15 33k ohm (orange-orange-orange-gold)
( ) R18 1.5m ohm (brown-green-green-gold)
( ) R20 360 ohm (orange-blue-brown-gold)
( ) R27 10k ohm (brown-black-orange-gold)

Install the following 1/4 watt, 1% tolerance resistors on the board. Solder and trim the leads.

( ) R16 32.4k ohm (orange-red-yellow-red-brown)
( ) R19 100k ohm (brown-black-black-orange-brown)

Note - Do not be concerned that there is no resistor in the R17 position.

Install and solder the following 10-pin SIP (single inline package) resistors noting the dot on the package is oriented toward pin 1 on the circuit board. Trim the leads.

( ) R1 1000 ohm SIP
( ) R21 4700 ohm SIP
( ) R22 4700 ohm SIP

Install and solder 12 - .1 uF monolithic capacitors at the following locations. Trim all leads.

( ) C7 .1 uF (104)
( ) C12 .1 uF (104)
( ) C13 .1 uF (104)
( ) C15 .1 uF (104)
( ) C16 .1 uF (104)
( ) C19 .1 uF (104)
( ) C20 .1 uF (104)
( ) C21 .1 uF (104)
( ) C25 .1 uF (104)
( ) C27 .1 uF (104)
( ) C28 .1 uF (104)
( ) C31 .1 uF (104)

Install 2 - 20pF ceramic capacitors at the following locations. Solder and trim the leads. (Note that 22pF capacitors may be supplied in the kit.)

( ) C17 20pF (20 or 200)
( ) C18 20pF (20 or 200)

Install 10 - 330pF mica capacitors at the following locations if supplied. Solder and then trim the leads. Note that these capacitors may not be necessary.

( ) C1 330pF (331)
( ) C2 330pF (331)
( ) C3 330pF (331)
( ) C4 330pF (331)
( ) C5 330pF (331)
( ) C6 330pF (331)
( ) C8 330pF (331)
( ) C9 330pF (331)
( ) C10 330pF (331)
( ) C11 330pF (331)

( ) Install a 1uF, 16 volt Tantalum capacitor at C14 observing polarity as indicated on the silk screen or component location diagram. The positive lead of the capacitor is the longer of the two capacitor leads and is also marked on the body of the capacitor. Trim the leads after soldering.

( ) Install and solder a 220 uF, 16 Volt, electrolytic capacitor at C22 observing proper polarity as indicated on the silk screen. The negative lead is indicated on the body of the capacitor. Trim the leads after soldering.

( ) Install and solder a 470 uF, 6.3 Volt electrolytic capacitor at C26 observing the proper polarity as indicated on the silk screen. The negative lead is indicated on the body of the capacitor. Trim the leads.

Install 5 - 1N4153 silicon diodes at the following locations observing polarity as indicated on the silk screen and component location diagram. There is a band at the cathode end of the diode. Solder and then trim the leads.

( ) CR5
( ) CR6
( ) CR7
( ) CR8
( ) CR9

Install and solder 4 red LEDs at the following locations observing the polarity as indicated on the silk screen or component location diagram. The cathode lead is shorter than the anode lead. Trim the leads after soldering.

( ) CR1
( ) CR2
( ) CR3
( ) CR4

Install and solder 2 - PN3645 transistors at the following locations:

( ) Q1
( ) Q2

( ) Take one of the DB25S connectors and slide the edge of the PC board between the rows of pins on the connector making sure that **all** the pins are centered over the fingers at the edge of the board at J1. This requires a bit of pushing but it will slide over the edge of the board. The connector should be fully seated and gripping the board snugly. Now solder the pins to the fingers.

( ) In a similar manner, install a DB25S connector at J2.

( ) In a similar manner, install a DB25S connector at J3.

( ) Install and solder a 16-pin, .1 inch spacing male DIP header at

location J4

( ) Install and solder a 2-pin, male header at the following locations:

( ) J7
( ) J12
( ) J13
( ) J14
( ) J15
( ) J16
( ) J17

( ) Install and solder a 6-pin, male header at J8

( ) Install and solder a 20-pin, .1 inch spacing male DIP header at location J9.

( ) Install and solder a 3-pin, male header at J10.

( ) Install and solder a 3-pin, male header at J11.

( ) Take the 4-terminal screw down type of terminal block and install and solder this 4-terminal power connector at J18 so that the wires enter the terminal block from the edge of the board.

( ) Install and solder the 8 position DIP switch at location S1 so that position 1 is oriented toward the notch on the silk screen.

( ) Install and solder the 4.9152 MHz. crystal at Y1 bending the leads so that the crystal lays flat against the PC board.

SWITCHING POWER SUPPLY ASSEMBLY

The following steps are only necessary if you are installing the on-board switching power supply to generate the +5 and -12 Volt supply voltages from a +10 to +12 Volt supply. If you are going to supply all the voltages from an off board power supply, skip the following steps until you come to the section titled, "Battery Installation."

( ) Check that all components in Group 4 of the TNC+ parts list are at hand.

( ) Position the TNC+ Issue 2, M2 circuit board on the working surface in front of you so that the silk screen printing is readable.

Install and solder the following IC sockets:

( ) U26 14-pin
( ) U27 14-pin

Install the following resistors in the indicated locations soldering and then trimming the leads.

( )	R23	1200 ohm, 1/4 watt, 5%	(brown-red-red-gold)
( )	R24	11k ohm, 1/4 watt, 5%	(brown-brown-orange-gold)
( )	R25	1 ohm, 1 watt, 5%	(brown-black-gold-gold)
( )	R26	10k ohm, 1/4 watt, 5%	(brown-black-orange-gold)
( )	R28	.1 ohm, 3 watt, 5%	
( )	R29	100 ohm, 1/4 watt, 5%	(brown-black-brown-gold)
( )	R30	47 ohm, 1/4 watt, 5%	(yellow-violet-black-gold)
( )	R31	3920 ohm, 1/4 watt, 1%	(orange-white-red-brown-brown)
( )	R32	1210 ohm, 1/4 watt, 1%	(brown-red-brown-brown-brown)

Install the following capacitors in the indicated locations, solder and trim the leads.

( ) C23 .1 uF, 100 Volt, Monolithic (104)
( ) C24 150 pF, 100 Volt, Mylar (151)
( ) C29 39 pF, 100 Volt, Ceramic (39 or 390)
( ) C30 150 pF, 100 Volt, Mylar (151)
( ) C33 .1 uF, 100 Volt, Monolithic (104)

( ) Install the 220 uF, 25 Volt electrolytic capacitor at C32 observing the polarity indicated on the silk screen and the component location diagram. Solder and trim the leads.

Install the following diodes at the following locations observing polarity as indicated on the silk screen and component location diagram. There is a band at the cathode end of the diode which should be at the same end as the bar on the diode symbol on the silk screen. Solder and trim the leads of each installed diode.

( ) CR10 MR854
( ) CR11 MR854
( ) CR12 1N4003

Note: The following step describes the installation of the 2N6126 transistor with a heat sink. The heat sink is only necessary if there is a need to supply substantial 5 Volt power to an off-board device. It should be possible to supply up to about 500mA. of current to an off-board device before needing the heat sink. The use of the VADCG external modem does not require a heat sink. Although the silk screen shows an outline for a small TO66 style heat sink, a TO220 style heat sink can also be used. Two screws and nuts are required for the TO66 style but only one set is needed for the TO220 style.

( ) Using a sharp knife, scrape away the solder resist on the back of the board around the heat sink mounting hole at Q3 which is closest to the edge of the board. The solder resist around this hole should be removed for a distance of about 1/8" in all directions to ensure electrical contact with the heat sink mounting hardware.

( ) Using needle nose pliers, bend the two outside leads of the TAB style 2N6126 transistor at right angles so that they fit into the two holes at location Q1 when the hole in the body of the transistor is centred over the larger hole near the bottom edge of the board. Cut off and discard the middle lead of the transistor. Insert the leads of the transistor into the holes in the heat sink and through the holes in the board and fasten the body of the transistor and heat sink to the board using the 4-40 nut with attached washer and 4-40 X 3/8 inch bolt provided. Solder and trim the leads.

( ) Using an Ohmmeter set to its lowest range, check for good contact between the tab of transistor Q3 (collector) and the cathode of CR11. Correct any poor contacts. Note that the collector connection is made through the heat sink mounting screw and so the screw and nut must be conductive. The internal lock washer can help to ensure good contact by digging into the metal of the screw, nut and land pattern.

( ) Using the length of #18 double enamelled wire provided (the larger diameter wire) wind 43 turns as evenly and closely as possible around one of the toroid cores to create an inductor of about 50 uH. Bring the lead to the final turn off the toroid about 1/2 inch from the lead to the first turn. Do not be concerned if you have to overlap some of the turns.

( ) Using the length of #22 double enamelled wire provided (the smaller diameter wire) wind 125 turns as evenly and closely as possible around a toroid core to create an inductor of about 480 uH. Bring the lead to the final turn off the toroid about 1/2 inch from the lead to the first turn. There will be a lot of overlapping of the turns.

( ) Place the 480 uH inductor at location L1 on the board with the leads coming off the left side. Cut the leads to a convenient length for soldering to the connection holes in the board and prepare the leads for soldering by scraping about 3/8 inch of enamel off the ends of each lead. Tin the ends of the leads and solder them in the connection holes. Pass a rubber 'mousetail' fastener over the edge of the toroid opposite the leads and insert the ends of the 'mousetail' through the two holes provided. Pull the ends of the 'mousetail' from

the bottom of the board so that the toroid is firmly fastened. A pair of pliers may be needed or very strong fingers are usually required to pull the 'mousetail' throught the board. Trim the excess length of mousetail close to the surface of the board.

( ) Push the two terminal posts provided into the two connection holes for L2 above CR11. Solder the posts onto the board.

( ) Place the 50 uH inductor at location L2 on the board with the leads coming off the side towards the terminal posts. Cut the leads to a convenient length for connection to the terminal posts and prepare the leads for soldering by scraping about 3/8 inch of enamel off the ends of each lead. Tin the ends of the leads and solder them to the terminal posts. Pass a rubber 'mousetail' fastener over the edge of the toroid opposite the leads and insert the ends of the 'mousetail' through the two holes provided. Pull the ends of the 'mousetail' from the bottom of the board so that the toroid is held securely and then trim the excess length close to the board.

( ) Read the section titled "Notes on Integrated Circuit Installation" following and insert the TL497 switching voltage regulator ICs into sockets at U26 and U27.

Battery installation

( ) Install and solder the 3.5 Volt Lithium battery at location B1 according to the polarity indicated by the silk screen on the board. Be extremely careful to not accidentally short out the leads of this battery since damage to the battery will result and there is a possibility that the battery may explode.

( ) Push the ends of a rubber 'mousetail' style tiedown through the two holes on either side of the battery at B1. Pull the ends of the 'mousetail' from the bottom side of the board to provide enough tension to hold the battery securely. After the battery has been installed you should be careful to avoid placing the PC board on a conducting surface which could short traces causing damage to the battery. Trim the length of 'mousetail' sticking below the bottom of the board.

( ) Check for solder bridges and cold solder joints. Re-solder if necessary.

( ) If you wish, now would be a good time to clean the rosin off the bottom of the board with an approved cleaner. This step is optional and normally not necessary.

Initial Checkout

( ) Using an accurate voltmeter, measure the voltage between ground (use the pin marked 'G' on the power connector) and the right hand pin of jumper header J17. You should find +3.3 Volts +/- Ø.2 Volts on this pin. If you do not get the proper reading, the problem may be a bad battery or improper installation of Q3, CR7 or B1. Correct any problem found before proceeding.

With On-board switching power supply.

If you have installed the on-board switching power supply components, do the following steps. If you have not installed the switching power supply, skip the following steps and do the steps in the section titled, "Without On-board switching power supply.'

( ) Prepare the leads of two wires providing the power to the TNC by stripping about 1/4" of insulation off the end of the leads. The screw-down terminals on the TNC board can accommodate a wide range of wire sizes.

( ) Using a small screwdriver, clamp the two power leads supplying the +1Ø to +15 Volt power to connector J18 terminals marked 'G' and '+12' observing proper polarity. The positive lead goes to the +12 terminal and the negative lead goes to the G (ground) terminal. (It is safer to make the connections when there is no power on the leads.) Note that no connections need be made to the terminals marked +5 and -12.

( ) Now we do the 'smoke test'. Apply power to the TNC+ and watch for any sign of smoke or the odour of something burning. If anything unusual is noticed, remove the power immediately and investigate and correct the problem before proceeding.

( ) With power applied, measure the applied Voltage between the +12 terminal and the G terminal of J18. It should be between +1Ø and +15 Volts but the TNC+ typically works with voltages as low as 7 and as high as 18 Volts. Note that there is a protective diode between the +12 and G terminals which will effectively short out any DC supply which is connected up backwards. Correct any problem found at this point before proceeding.

The measured value is _____ Volts.

( ) Measure the Voltage between the G terminal and the -12 terminal. It should be between -11 and -13 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is _____ Volts.

( ) Using an accurate Voltmeter, measure the Voltage between the G terminal and the +5 terminal. It should be between +5.Ø and +5.2 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is _____ Volts.

( ) Remove DC power from the TNC+ and proceed to the section titled, 'Notes on Integrated circuit installation'.

Without on-board Switching Power Supply

If you are using your own off-board power supply to provide the regulated voltages required for operation of the TNC+ and are not using the on-board switching power supply, do the following steps. If you are using the on-board supply you should have done the steps in the section titled, 'With on-board switching power supply' above.

Note: If you are supplying your own power supply, it should provide the following regulated Voltages and tolerances.

+5 Volts +/- .2 Volts
+12 Volts +/- 2 Volts
-12 Volts +/- 1 Volt

( ) Prepare the leads of the four wires coming from the external power supply by stripping about 1/4" of insulation off the end of the leads. The screw-down terminals on the TNC board can accommodate a wide range of wire sizes.

( ) Using a small screwdriver, clamp the power supply leads to the appropriate terminals of J18. (It is safer to make the connections when there is no power on the leads.)
( ) Now we do the 'smoke test'. Apply power to the TNC+ and watch for any sign of smoke or the odour of something burning. If anything unusual is noticed, remove the power immediately and investigate and correct the problem before proceeding.

( ) With power applied, measure the applied Voltage between the +12 terminal and the G terminal of J18. It should be between +10 and +15 Volts. Note that there is a protective diode between the +12 and G terminals which will effectively short out any DC supply which is connected up backwards. Correct any problem found at this point before proceeding.

The measured value is _____ Volts.

( ) Measure the Voltage between the G terminal and the -12 terminal. It should be between -11 and -13 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is _____ Volts.

( ) Using an accurate Voltmeter, measure the Voltage between the G terminal and the +5 terminal. It should be between +5.0 and +5.2 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is _____ Volts.

( ) Remove DC power from the TNC+ and proceed to the section titled, 'Notes on Integrated circuit installation'.

Notes on Integrated circuit installation

Some of the ICs such as the 6264LP-15s are sensitive to static discharge. Special precautions may need to be taken when handling these ICs to avoid damage. If you are handling them in an environment with low humidity or otherwise have a static electricity problem. Make sure that everything that the ICs come in contact with is at the same electrostatic potential.

ICs should be inserted so that pin 1 is at the end indicated by the notch on the silk screen or component layout diagram. Pin one is usually indicated by a groove or notch in the centre of one end of the IC and/or by a shallow circle next to pin 1. Take special care because all ICs on this board are not oriented in the same direction.

It is best to insert ICs with special IC insertion tools but it may be done by hand with a little care. If done by hand, it may be necessary to press the sides of some of the ICs against a flat surface to bend the leads so that they are parallel to each other to align with the socket holes. The pins on ICs shipped from the factory are usually splayed out slightly to work better in insertion tools. When inserting ICs, make sure that the ends of the pins are in the socket holes and then apply a firm pressure with the thumb and forefinger of both hands to push and seat the IC in its socket. Push it down so that all pins go in at the same time. Do not try to insert one end or side before the other.

( ) Look for any bent pins on all the ICs. Carefully straighten any bent pins that are discovered. Needle nose pliers may be used for this.

Insert the following ICs into the indicated sockets:

( ) U1 1488
( ) U2 1489
( ) U3 1489
( ) U4 1489
( ) U5 1488
( ) U6 8273
( ) U7 8255
( ) U8 8250
( ) U9 7406
( ) U10 74LS138
( ) U11 4024
( ) U12 4040
( ) U13 74LS138
( ) U14 8085
( ) U15 74LS373
( ) U16 74LS00
( ) U17 8212
( ) U18 2764

( ) U19 6264
( ) U20 6264
( ) U21 6264
( ) U22 6264
( ) U23 6264
( ) U24 6264
( ) U25 6264

( ) Check all the pins on all the ICs which have been inserted to verify that they have gone straight into the holes on the sockets. Sometimes a pin gets folded under the IC during insertion or misses the hole in the socket entirely. Correct any problems discovered.

NOTE: ICs may be removed by inserting the tip of a small screwdriver between the end of the IC and its socket and twisting and prying the IC out of the socket. Only lift the IC a little at a time from each end so that the IC remains parallel to the socket as it is being removed. A tapered staple remover is a good tool to remove the wider ICs if you have one.

( ) Check all the ICs to see that pin 1 is correctly oriented according to the silk screen or component location diagram. Remove and re-insert any incorrectly oriented ICs.

( ) Now we do another 'smoke test'. Reapply power to the TNC+ and watch for any sign of smoke or the odour of something burning. If anything unusual is noticed, remove the power immediately and investigate and correct the problem before proceeding.

( ) Measure the applied Voltage between the +12 terminal and the G terminal of J18. It should be between +10 and +15 Volts. Note that there is a protective diode between the +12 and G terminals which will effectively short out any DC supply which is connected up backwards. Correct any problem found at this point before proceeding.

The measured value is 11.90 Volts.

( ) Measure the Voltage between the G terminal and the -12 terminal. It should be between -11 and -13 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is -12.02 Volts.

( ) Using an accurate Voltmeter, measure the Voltage between the G terminal and the +5 terminal. It should be between +5.0 and +5.2 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

The measured value is 5.10 Volts.

( ) Using an accurate Voltmeter, measure the Voltage between the G terminal and pin 26 of any of the memory ICs. It should be between +5.0 and +5.2 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

( ) Using an accurate Voltmeter, measure the Voltage between the G terminal and the right hand terminal of J17. It should be between +5.Ø and +5.2 Volts. If the Voltage is not in this range, diagnose the problem and correct it before proceeding.

( ) Remove power from the TNC. The basic testing of the TNC has been completed.

FINAL MOUNTING OF TNC+

At the present time, the cabinet kit for the TNC+ is not available. The TNC+ board should be mounted in a metal enclosure and should be well-grounded and shielded for reliable operation especially when the unit will be operating in an area of high RF potential or near the antenna of a radio receiver.

Connector J1Ø should be connected to a SPST pushbutton mounted on the enclosure to provide a reset function switch capability. The TNC+ is automatically reset when powered up so this remote reset switch may not be necessary in all environments.

A trap switch using a SPDT pushbutton may also be mounted on the enclosure and connected to J11 as follows:

Pin 1 goes to the normally closed contact.
Pin 2 goes to the common connection.
Pin 3 goes to the normally open contact.

Depression of the pushbutton will cause a 'TRAP' or non-maskable interrupt to be generated. What this interrupt will do depends on the software package installed in the TNC but usually causes the TNC+ status to be stored and the monitor program to be invoked. This is normally used in debugging and analyzing software problems when they occur.

Connector J11 can be used to connect up the 4 LED indicators which can be mounted remotely on the enclosure or other convenient location. Pin 1 of this connector should go to the anodes of all the LEDs and one of pins 2 through 5 should go to each of the cathodes of the LEDs. The meaning of each of the LEDs is determined by the software package running in the TNC+.

OPERATION

The operational details of the TNC+ depend entirely on the software and firmware package that is being used. This information will be included with the software package. It is expected that there will be a number of sources of software for this board.

CONFIGURATION

The wiring and basic testing of the TNC has been completed. Because of the flexible design of the TNC, there are several jumpers and switches that must be installed to configure the TNC for the particular environment in which it will be used. This section describes how to set it up for most environments.

Terminal Configuration

Socket J6 is to be plugged with a 16-pin header (component carrier) provided in the kit. If you are connecting the TNC+ to a standard terminal it should be wired as a DCE straight across as follows:

Connect pin 1 to pin 16
Connect pin 2 to pin 15
Connect pin 3 to pin 14
Connect pin 4 to pin 13
Connect pin 5 to pin 12
Connect pin 6 to pin 11
Connect pin 7 to pin 10
Connect pin 8 to pin 9

If you are interfacing the TNC to a device which expects a terminal to be connected to it, the header should be wired as a DTE as follows:

Connect pin 1 to pin 15
Connect pin 2 to pin 16
Connect pin 3 to pin 11
Connect pin 4 to pin 10
Connect pin 5 to pin 9
Connect pin 6 to pin 14
Connect pin 7 to pin 13
Connect pin 8 to pin 12

If you are not using a standard DTE or DCE configuration you may wire up the header according to your interface requirements.

Memory Configuration

Jumper positions J12 through J17 control the memory configuration and write protect RAM features. They should be plugged according to the type of memory installed in sockets U18 - U25. Three configurations are possible.

A. 2764 in U18, 6264s in U19-U25.
B. 2764s in U18-U19, 6264s in U20-U25.
C. 2764s in U18-U21, 6264s in U22-U25.

Configuration A gives 8K bytes of EPROM and 56K bytes of RAM.
Configuration B gives 16K bytes of EPROM and 48K bytes of RAM.
Configuration C gives 32K bytes of EPROM and 32K bytes of RAM.

Four shorting plugs should be installed to give the three possible memory configurations as follows:

Configuration A - Install J14, J15, J16 and J17
Configuration B - Install J12, J13, J16 and J17
Configuration C - Install J12, J13, J14 and J15

Write Protect

In memory configurations A and B certain blocks of RAM may be write protected by removing certain shorting blocks. Note that addresses are in hexadecimal tbase 16).

Configuration A
Remove J16 to write protect RAM from 2000H to 7FFFH.
Remove J14 to write protect RAM from 2000H to 3FFFH.

Configuration B
Remove J16 to write protect RAM from 4000H to 7FFFH.

Modem Configuration

Socket J5 is to be plugged with a 14-pin header (component carrier) provided in the kit. This header can be wired for asynchronous as well as synchronous self clocking) modems. All common configurations are wired straight accross:

Asynchronous Modem (most common)
Connect pin 2 to pin 13
Connect pin 7 to pin 8
Connect pin 4 to pin 11

Synchronous Modem (supplying both receive and transmit clocking)
Connect pin 1 to pin 14
Connect pin 3 to pin 12
Connect pin 6 to pin 9

Synchronous Modem (supplying only receive clocking)
Connect pin 1 to pin 14
Connect pin 3 to pin 12
Connect pin 7 to pin 8

Modem Baud rate selection

The clocking signals for the 8273 are controlled by jumper selection on J9. Connect pin 20 to the pin which delivers the clock speed matching the desired Baud rate. Connect pin 1 to the pin which delivers a clock speed of 32 times the desired Baud rate. For example, the most common selection is for a 1200 Baud asynchronous modem of the Bell 202 type. This is done by connecting the following pins on J9.

Connect pin 1 (32X clock) to pin 15 (38,400Hz.)
Connect pin 20 (1X clock) to pin 2 (1200Hz.)

8255 Interrupt Control

Jumper position J1Ø controls the operation of interrupts from the 8255A Programmable Peripheral Interface. When using software which does not support the 8255 interrupts you must jumper pin 1 to pin 2 in order to ensure that no interrupts are generated by the 8255. (Currently, most software does not support 8255 interrupts.) When there are no connections made to any of the pins on J1Ø, Interrupts via RST 7 are generated by the INTRa line on the 8255A. Interrupts from the 8255 INTRa and INTRb lines are generated when pin 2 is jumpered to pin 3 on J1Ø. For details on the use and control of interrupts generated by the 8255, consult the manufacturer's specification sheet.

TROUBLESHOOTING

The following information comes from feedback from the field on problems encountered with getting the TNC+ operational. Please feel free to write about any problems you have encountered as this feedback is a considerable help in improving the product.

1. Failure of the collector of Q3 to make proper contact through the heat sink mounting hardware may be evidenced by resistor R30 getting excessively hot and a failure of the 5 Volt switching power supply. R30 may get so hot that it will become charred. The procedure outlined in the memorandum of February 12, 1986 for page 19 of the preliminary assembly instructions should correct this problem and the change in the assembly instructions should prevent this problem from re-occurring.

2. The value for resistor R13 was incorrectly specified as either 4.1K or 4700 ohms. This resistor must be changed to 270 ohms. This will correct a problem which results in data in RAM memory being changed when the TNC+ is powered of and on.

3. The 5 Volt supply tolerances have been tightened to +5.0 to +5.2 Volts instead of +4.8 to +5.2 Volts. This has been done to avoid any potential problem with interaction with the voltage comparator which may be set for too high a Voltage. To increase the output voltage of the switching power supply either increase the value of R31 or decrease the value of R32. To decrease the output voltage - either decrease the value of R31 or increase the value of R32.

4. Resistor R16 is used to trim the switching voltage of the comparator U17. This comparator is used to reset the microprocessor and disable writes to RAM memory when the power supply voltage drops to a level that is too low for the microprocessor to operate at. If RAM memory is being changed when the TNC+ is being powered on or off, it may be that the comparator switching voltage is incorrect. (First make sure that R13 is the correct value!) Usually it is unnecessary to install this trimming resistor and it must be field selected if added. In order to measure the comparator switching Voltage you will need an accurate voltmeter and a variable voltage power supply. The procedure is as follows: Power the TNC+ using the variable Voltage supply and measure the voltage present on line CS2 (the collector of Q1). You should have about 5 Volts on the CS2 line. Now reduce the supply voltage very slowly until the voltage on CS2 suddenly drops to 0. Now measure the voltage on the +5 pin of the power connector. This is the comparator switching voltage. It should be between 4.5 and 4.75 Volts. If it is below 4.5 Volts, you may increase it by putting a trimming resistor at R16. You will have to adjust the voltage by trial and error depending on how much you need to move. Do not increase the comparator switching voltage above 4.75 Volts. If for some reason it is above 4.75 volts without R16 you must either increase the value of R17 or decrease the value of R19.

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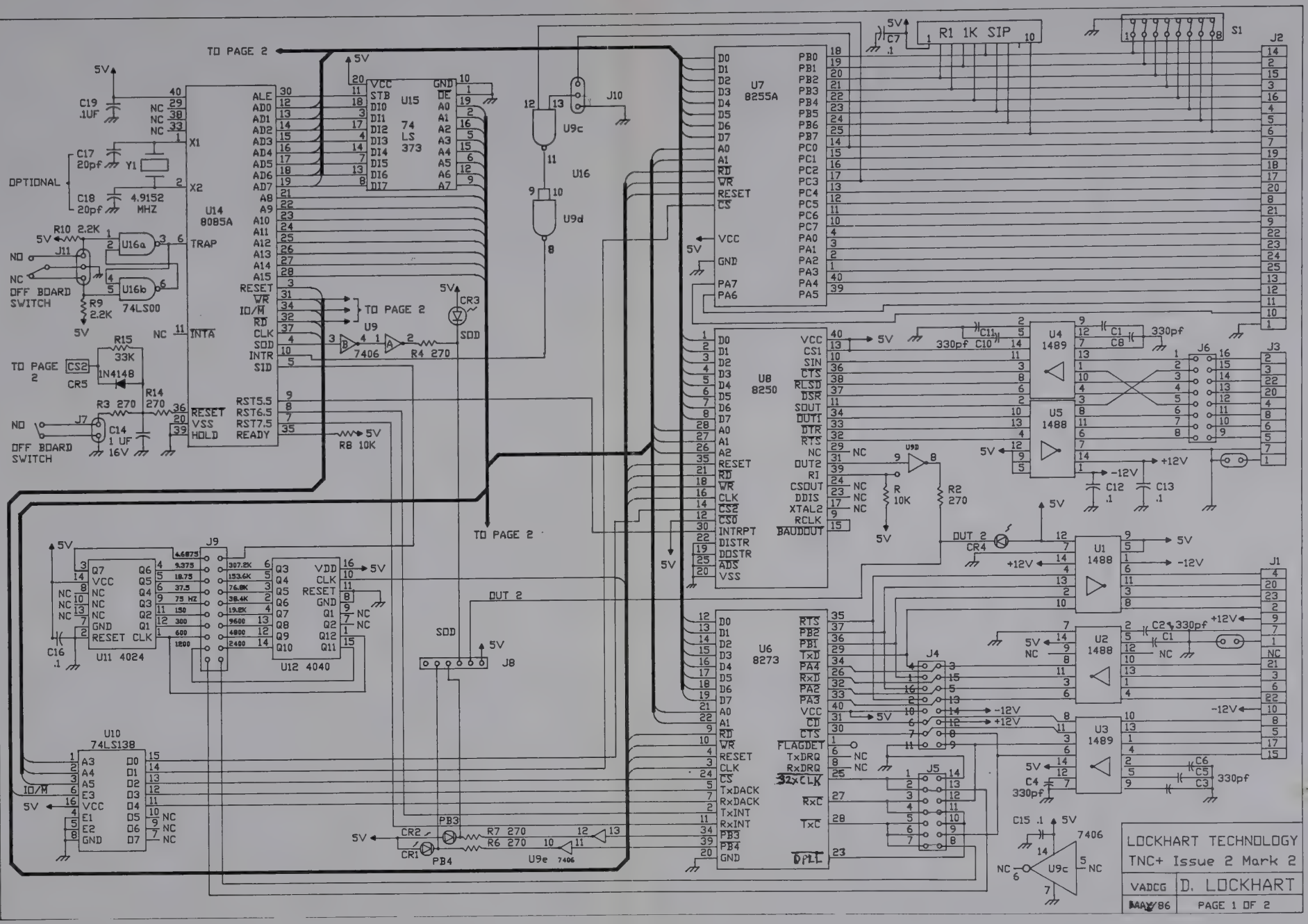
TO PAGE 2
U14 8085A
U15 74 LS 373
U7 8255A
U8 8250
U6 8273
U9 7406
U10 74LS138
U11 4024
U12 4040
U4 1489
U5 1488
U1 1488
U2 1488
U3 1489
R1 1K SIP
S1
J1
J2
J3
J4
J5
J6
J7
J8
J9
J10
J11
X1
Y1
4.9152 MHZ
OPTIONAL
OFF BOARD SWITCH
74LS00
1N4148
CR1
CR2
CR3
CR4
CR5
DUT 2
SDD
PB3
PB4
LOCKHART TECHNOLOGY
TNC+ Issue 2 Mark 2
VADCG
D. LOCKHART
MAY 86
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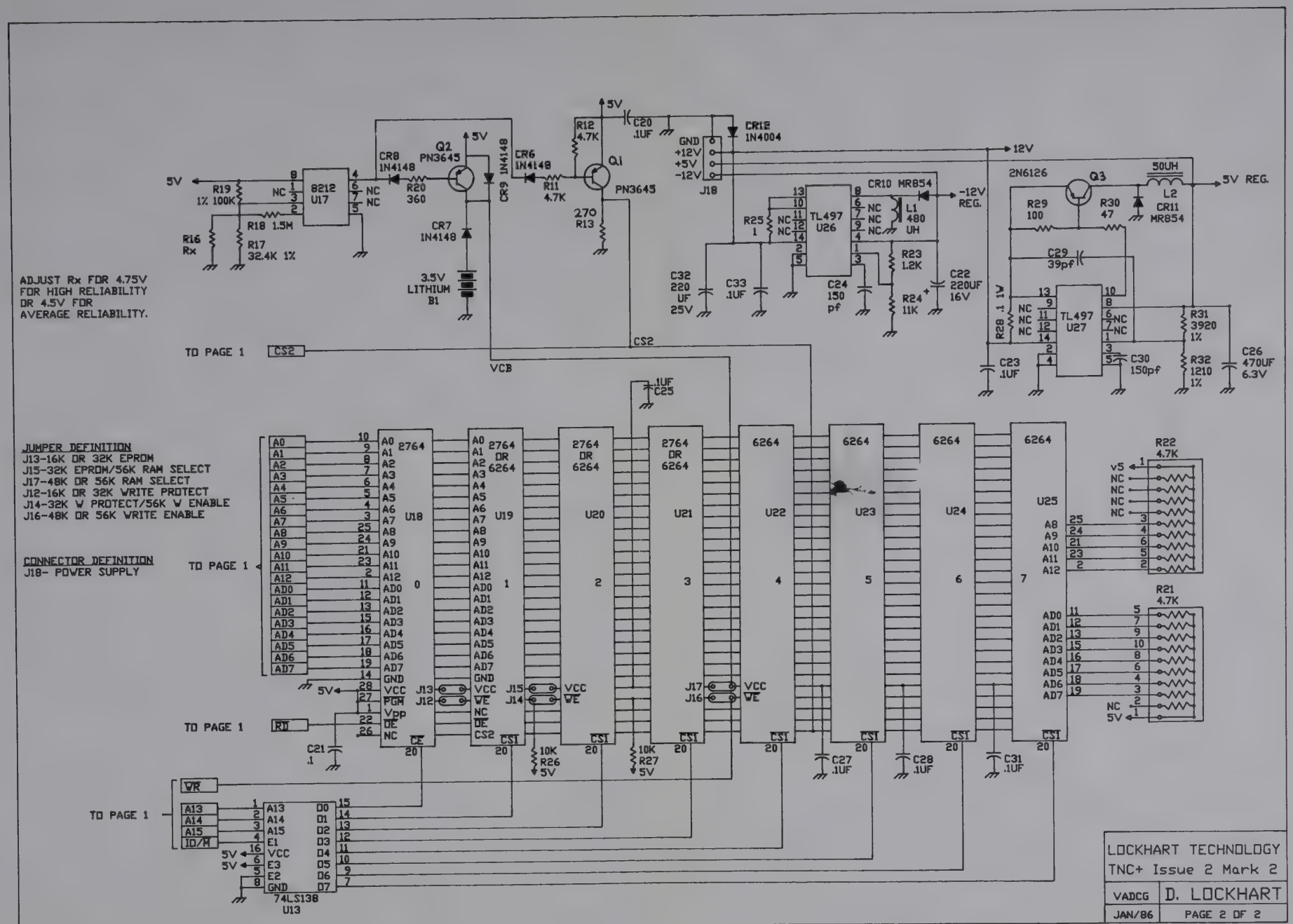
ADJUST Rx FOR 4.75V FOR HIGH RELIABILITY OR 4.5V FOR AVERAGE RELIABILITY.
JUMPER DEFINITION
J13-16K OR 32K EPROM
J15-32K EPROM/56K RAM SELECT
J17-48K OR 56K RAM SELECT
J12-16K OR 32K WRITE PROTECT
J14-32K W PROTECT/56K W ENABLE
J16-48K OR 56K WRITE ENABLE
CONNECTOR DEFINITION
J18- POWER SUPPLY
TO PAGE 1
CS2
VCB
RD
WR
5V
12V
-12V
5V REG.
-12V REG.
R19 1% 100K
R18 1.5M
R16 Rx
R17 32.4K 1%
8212 U17
CR8 1N4148
CR6 1N4148
CR9 1N4148
CR7 1N4148
Q2 PN3645
Q1 PN3645
R20 360
R11 4.7K
R12 4.7K
270 R13
3.5V LITHIUM B1
C20 .1UF
C25 .1UF
CR1E 1N4004
J18
TL497 U26
CR10 MR854
L1 480 UH
R25 1
R23 1.2K
R24 11K
C22 220UF 16V
C32 220 UF 25V
C33 .1UF
C24 150 pf
2N6126
Q3
50UH
L2
CR11 MR854
R29 100
R30 47
C29 39pf
R28 .1 1W
TL497 U27
C23 .1UF
C30 150pf
R31 3920 1%
R32 1210 1%
C26 470UF 6.3V
2764 U18
2764 DR 6264 U19
2764 DR 6264 U20
2764 DR 6264 U21
6264 U22
6264 U23
6264 U24
6264 U25
R22 4.7K
R21 4.7K
C21 .1
C27 .1UF
C28 .1UF
C31 .1UF
R26 10K 5V
R27 10K 5V
74LS138 U13
LOCKHART TECHNOLOGY
TNC+ Issue 2 Mark 2
VADCG
D. LOCKHART
JAN/86
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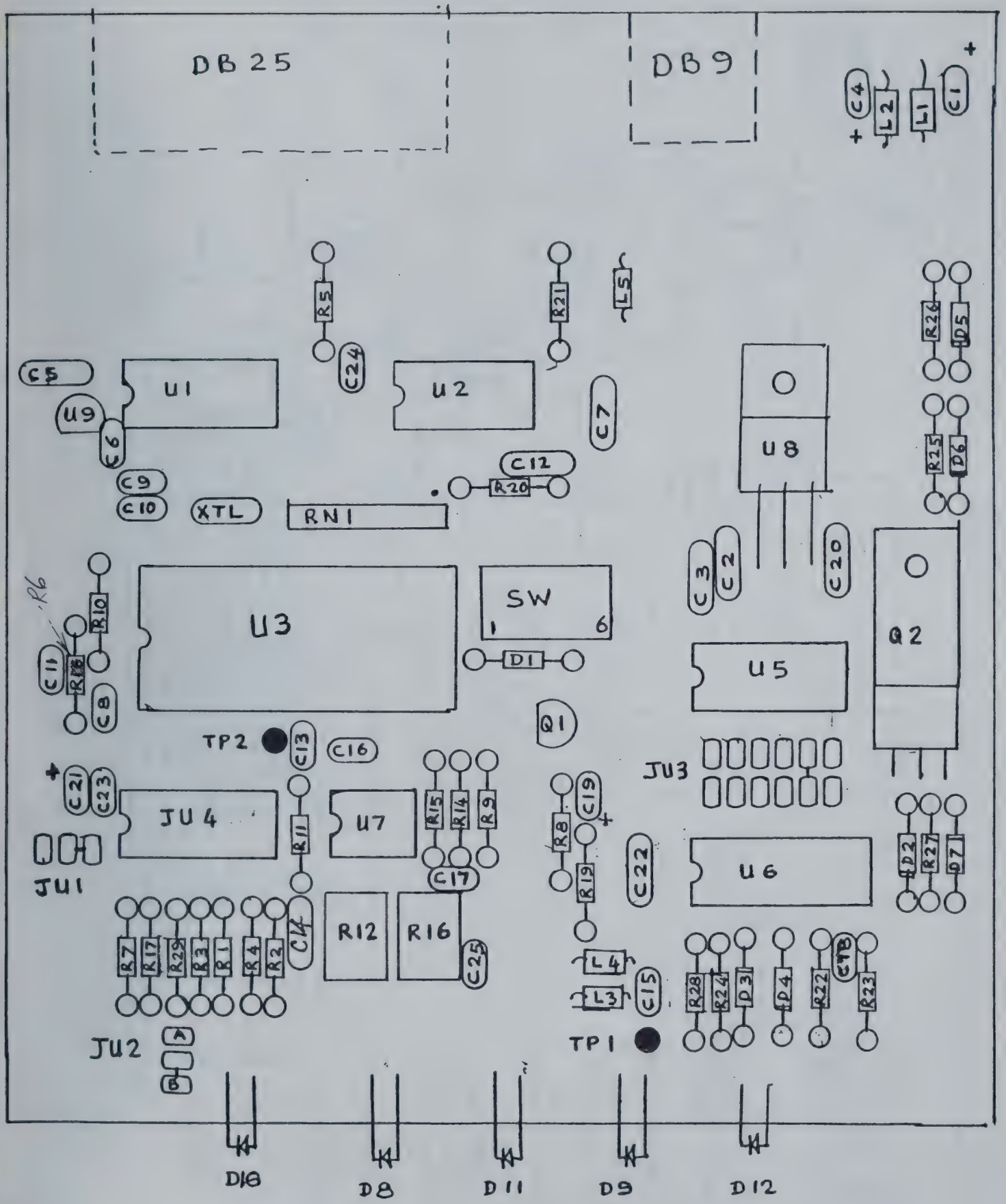
Component Designation	Qty	Value	Description
*Resistors			
R1,2,3,4,28	5	470 ohm	All 1/4-W, 5% Resistors:
R5	1	1 K	
R7,15,17,19, + 29	5	4.7 K	
R6	1	7.2 K	
R11,21	2	18 K	
R9,14	2	47 K	
R20,23,27	3	10 K	
R26	1	27 K	
R8,22,24	3	100 K	
R25	1	470 K	
R10	1	1 M	
R12,13	2	10 K	Multiturn Trimmer, Vertical Mount
RN1	1	4.7 K	SIP Resistance Network
R18			<not used>
*Integrated Circuits			
U1	1	1488	Quad Line Driver
U2	1	1489	Quad Line Driver
U3	1	AMD7910	AMD World Chip Modem
U4	1	74CH86 or 74LS86	Quad 2-input Exclusive-OR
U5	1	4025	3-input NOR gate (MC14025)
U6	1	4521	24-stage frequency divider (MC14521)
U7	1	1458	Dual Op Amp (MC1458)
U8	1	7805	+5V Fixed Output Regulator
U9	1	79L05	-5V Fixed Output Regulator
*Transistors			
Q1	1	2N3904	NPN switching transistor
Q2	1	VN89AF	N-Channel VMOS FET
*Capacitors			
C1,4,21	3	10uF/25V	Tantalum, 0.1" lead spacing
C19	1	4.7uF/25V	" " " "
C2,3,5,20,22	5	0.33uF/50V	Ceramic, 0.2" lead spacing
C6,11,13,15, +16,17,23,24	8	0.1 uF/50V	" 0.1" " "
C12	1	.022uF/50V	" " " "
C8,18	2	.001uF/50V	10% " " " "
C14,25	2	470pF/50V	" " " "
C7	1	390pF/50V	" " " "
C9,10	2	10pF/50V	" " " "

Component Designation	Qty	Value	Description
*Diodes			
D1,3,4,5,6	5	1N4148	Signal Diode, silicon
D2	1	1N60	Signal Diode, germanium
D7	1	1N4005	Silicon Rectifier
D8,9,10,11,12	5	LED	Light Emitting Diodes
*Switches			
S1-6	1		6-position DIP switch
*Crystals			
XTL	1	2.4576-MHz	HC-18, Crystal
*Connectors			
DB-25	1		Connector, PC Edge Mount
DB-9	1		Connector, PC Edge Mount
*Chokes			
L1,2,3,4,5	5		Ferrite Bead Chokes, 2 turns
*Sockets			
8-pin	1		IC Sockets
14-pin	4		
16-pin	1		
28-pin	1		


DB 25
DB 9
C4
L2
L1
C1
R5
C24
R21
L5
R26
D5
C5
U1
U2
C7
U8
U9
C6
C12
R20
R25
D6
C9
C10
XTL
RN1
C3
C2
C20
SW
1
6
U3
R10
R6
C11
R16
C8
D1
Q2
U5
Q1
TP2
C13
C16
JU3
C21
C23
JU4
U7
R15
R14
R9
C19
R8
R19
C22
U6
JU1
C17
R12
R16
C14
R7
R17
R29
R3
R1
R4
R2
C25
L4
L3
C15
R28
R24
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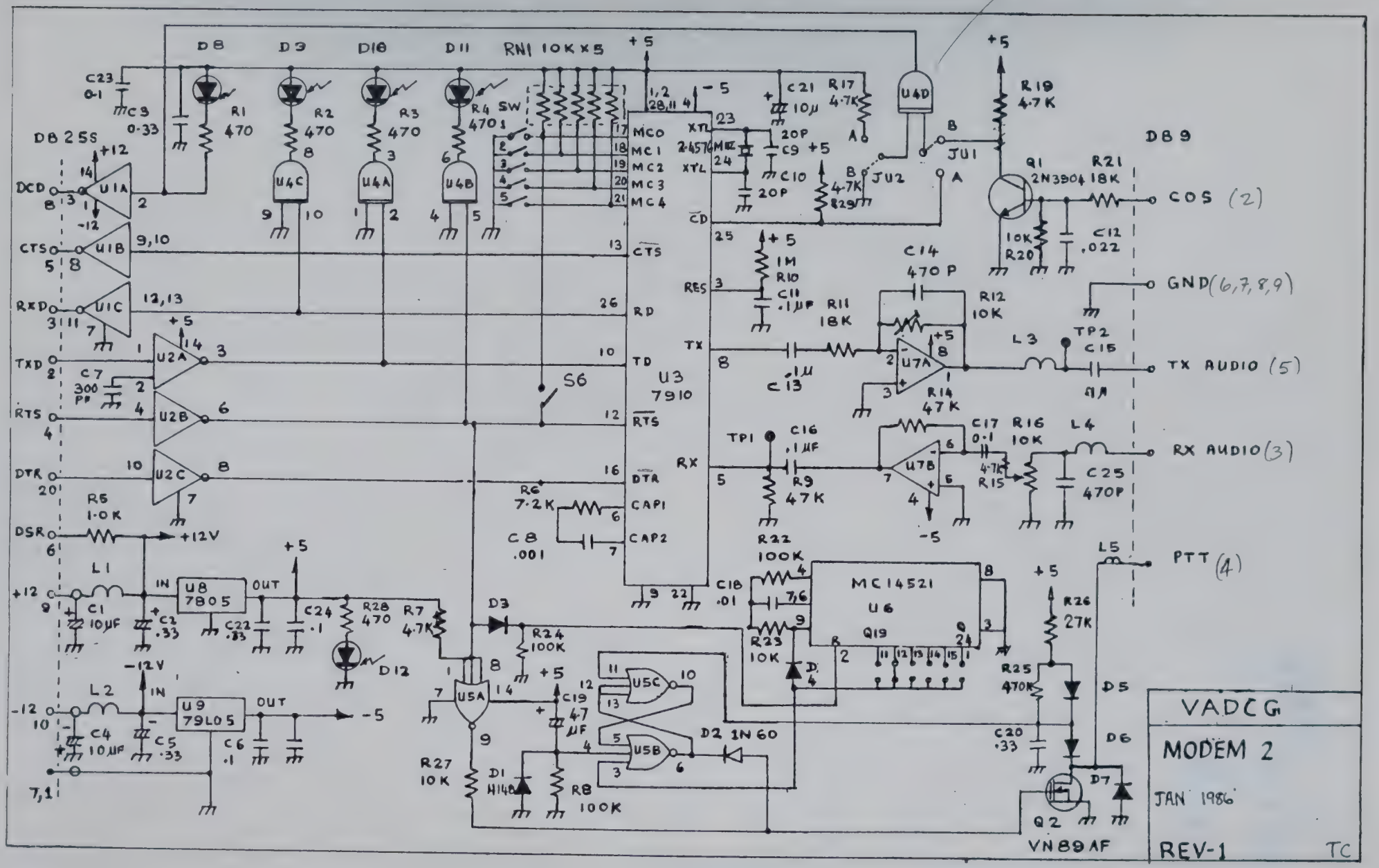
D7
JU2
TP1
D10
D8
D11
D9
D12


JU1 - A
JU2 - B
INT MODEM
DB25S
DB9
U3 7910
U1A
U1B
U1C
U2A
U2B
U2C
U4A
U4B
U4C
U4D
U5A
U5B
U5C
U6 MC14521
U7A
U7B
U8 7805
U9 79L05
RN1 10K x 5
SW
S6
JU1
JU2
Q1 2N3904
Q2 VN89AF
D1 H11A1
D2 1N60
D3
D4
D5
D6
D7
D12
TP1
TP2
L1
L2
L3
L4
L5
R1 470
R2 470
R3 470
R4 470
R5 1.0K
R6 7.2K
R7 4.7K
R8 100K
R9 47K
R10 1M
R11 18K
R12 10K
R14 47K
R15 4.7K
R16 10K
R17 4.7K
R19 4.7K
R20 10K
R21 18K
R22 100K
R23 10K
R24 100K
R25 470K
R26 27K
R27 10K
R28 470
R29 4.7K
C1 10µF
C2 .33
C4 10µF
C5 .33
C6 .1
C7 300 PF
C8 .001
C9 20P
C10 20P
C11 .1µF
C12 .022
C13 .1µ
C14 470 P
C15 .01
C16 .1µF
C17 0.1
C18 .01
C19 47 µF
C20 .33
C21 10µ
C22 .33
C23 0.1
C24 .1
C25 470P
+5
-5
+12
-12
+12V
-12V
COS (2)
GND (6,7,8,9)
TX AUDIO (5)
RX AUDIO (3)
PTT (4)
DCD
CTS
RXD
TXD
RTS
DTR
DSR
MC0
MC1
MC2
MC3
MC4
XTL
CD
RES
TX
RD
TD
RTS
RX
DTR
CAP1
CAP2
VADCG
MODEM 2
JAN 1986
REV-1
TC

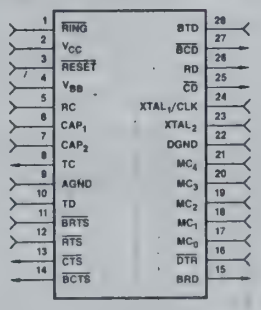
Am7910

FSK MODEM
WORLD-CHIP™
PRELIMINARY DATA (Revised)

DISTINCTIVE CHARACTERISTICS

- Complete FSK MODEM in a 28-pin package – just add line interface
- Compatible with Bell 103/113/108, Bell 202, CCITT V.21, CCITT V.23 specifications
- No external filtering required
- All digital signal processing, digital filters and ADC/DAC included on-chip
- Includes essential RS-232/CCITT V.24 handshake signals
- Auto-answer capability
- Local copy/test modes
- 1200 bps full duplex on 4-wire line
- Pin-programmable mode section

Figure 1. Connection Diagram



01238C-1

GENERAL DESCRIPTION

The Am7910 is a single-chip asynchronous Frequency Shift Keying (FSK) voiceband modem. It is pin selectable for baud rates of 300, 600 or 1200 bits per second and is compatible with the applicable Bell and CCITT recommended standards for 103/113/108, 202, V.21 and V.23 type modems. Five mode control lines select a desired modem configuration.

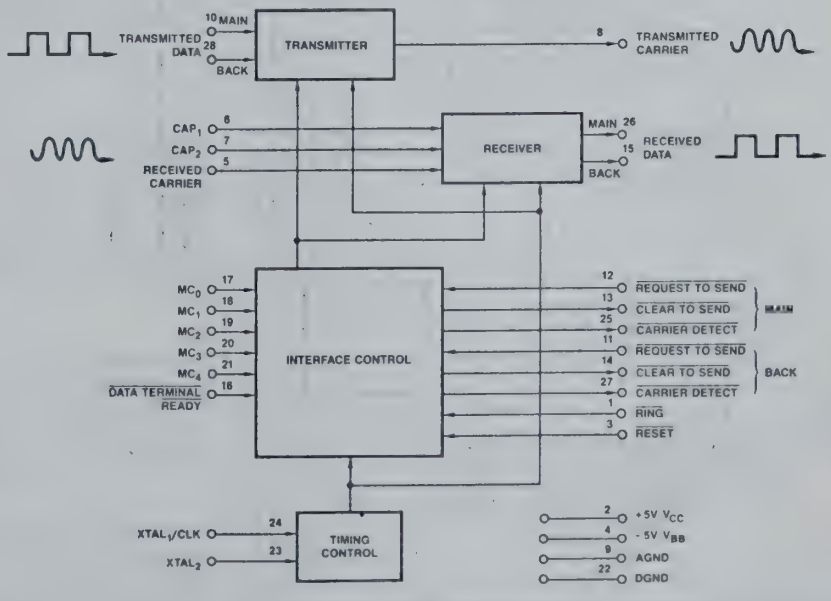
Digital signal processsing techniques are employed in the Am7910 to perform all major functions such as modulation, demodulation and filtering. The Am7910 contains on-chip analog-to-digital and digital-to-analog converter circuits to minimize the external components in a system. This device includes the essential RS-232/CCITT V.24 terminal control signals with TTL levels.

Clocking can be generated by attaching a crystal to drive the internal crystal oscillator or by applying an external clock signal.

A data access arrangement (DAA) or acoustic coupler must provide the phone line interface externally.

The Am7910 is fabricated using N-channel MOS technology in a 28-pin package. All the digital input and output signals (except the external clock signal) are TTL compatible. Power supply requirements are ±5 volts.

Figure 2. Am7910 Block Diagram



01238C-2

INTERFACE SIGNAL DESCRIPTION

MC_0-MC_4 (CONTROL INPUTS)

These five inputs select one of thirty-two modem configurations according to the Bell or CCITT specifications listed in Table 1. Only 19 of these 32 modes are actually available to the user.

Modes 0-8 are the normal operation modes. The 1200 Baud modes can be selected with or without a compromise equalizer.

Modes 16-25 permit loop back of the Am7910 transmitter and receiver. No internal connection is made. The user must externally connect the TRANSMITTED CARRIER pin (Figure 3) to the RECEIVED CARRIER pin if analog loopback is required. For digital loopback, external connection of RECEIVED DATA and TRANSMITTED DATA is required. Whenever a mode in this group is selected, the effect is to set all transmit and receive filters to the same channel frequency band so that loopback can be performed.

Modes 9-15 and 26-31 are reserved and should not be used.

DATA TERMINAL READY ($\overline{DTR}$)

A LOW level on this input indicates the data terminal desires to send and/or receive data via the modem. This signal is gated with all other TTL inputs and outputs so that a low level enables all these signals as well as the internal control logic to function. A HIGH level disables all TTL I/O pins and the internal logic.

REQUEST TO SEND ($\overline{RTS}$)

A LOW level on this input instructs the modem to enter transmit mode. This input must remain LOW for the duration of data transmission. The signal has no effect if $\overline{DATA\ TERMINAL\ READY}$ is HIGH (disabled). A HIGH level on this input turns off the transmitter.

CLEAR TO SEND ($\overline{CTS}$)

This output goes LOW at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes LOW. Actual data to be transmitted should not be presented to the TRANSMITTED DATA input until a LOW is indicated on the $\overline{CLEAR\ TO\ SEND}$ output. Normally the user should force the TD input HIGH whenever $\overline{CTS}$ is off (HIGH). This signal never goes LOW as long as $\overline{DTR}$ is HIGH (disabled). $\overline{CLEAR\ TO\ SEND}$ goes HIGH at the end of a delay initiated when $\overline{REQUEST\ TO\ SEND}$ goes HIGH.

CARRIER DETECT ($\overline{CD}$)

A LOW on this output indicates that a valid carrier signal is present at the receiver and has been present for at least a time, t_{CDON}, where t_{CDON} depends upon the selected modem configuration (Table 2). A HIGH on this output signifies that no valid carrier is being received and has not been received for a time, t_{CDOFF}. $\overline{CARRIER\ DETECT}$ remains HIGH when $\overline{DTR}$ is HIGH. Values for t_{CDON} and t_{CDOFF} are configuration dependent and are listed in Table 2.

TRANSMITTED DATA (TD)

Data bits to be transmitted are presented on this input serially; HIGH (mark) corresponds to logic 1 and LOW (space) corresponds to logic 0. This data determines which frequency appears at any instant at the TRANSMITTED CARRIER output pin (Table 2). No signal appears at the TRANSMITTED CARRIER output unless $\overline{DTR}$ is LOW and $\overline{RTS}$ is LOW.

RECEIVED DATA (RD)

Data bits demodulated from the RECEIVED CARRIER input are available serially at this output; HIGH (mark) indicates logic 1 and LOW (space) indicates logic 0. Under the following conditions this output is forced to logic 1 because the data may be invalid:

1. When $\overline{CARRIER\ DETECT}$ is HIGH
2. During the internal squelch delay at half-duplex line turn around (202/V.23 modes only)
3. During soft carrier turnoff at half-duplex line turn around (202 mode only)
4. When $\overline{DTR}$ is HIGH
5. When $\overline{RTS}$ ON and $\overline{BRTS}$ OFF in V.23/202 modes only
6. During auto-answer sequence

BACK REQUEST TO SEND ($\overline{BRTS}$)

Since the 1200 bps modem configurations, Bell 202 and CCITT V.23, permit only half duplex operation over two-wire lines, a low baud rate "baokward" channel is provided for transmission from the main channel receiver to the main channel transmitter. This input signal ($\overline{BRTS}$) is equivalent to $\overline{REQUEST\ TO\ SEND}$ for the main channel, except it belongs to the backward channel. Note that since the Am7910 contains a single transmitter, $\overline{RTS}$ and $\overline{BRTS}$ should not be asserted simultaneously. $\overline{BRTS}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. In all other modes it is ignored.

For V.23 mode the frequency appearing at the transmitted carrier (TC) output pin is determined by a MARK or SPACE at the back transmitted data (BTD) input (Table 2).

For 202 mode a frequency of 387Hz appears at TC when $\overline{BRTS}$ is LOW and BTD is HIGH. No energy (0.0 volts) appears at TC when $\overline{BRTS}$ is HIGH. BTD should be fixed HIGH for 202 back channel transmission. The signal, $\overline{BRTS}$, then is equivalent to the signal, Secondary Request-to-Send, for 202 S/T modems, or Supervisory Transmitted Data for 202 C/D modems.

BACK CLEAR TO SEND ($\overline{BCTS}$)

This line is equivalent to $\overline{CLEAR\ TO\ SEND}$ for the main channel, except it belongs to the back channel. $\overline{BCTS}$ is meaningful only when a V.23 mode is selected by MC_0-MC_4. This signal is not used in Bell 202 back mode.

BACK CARRIER DETECT ($\overline{BCD}$)

This line is equivalent to $\overline{CARRIER\ DETECT}$ for the main channel, except it belongs to the backward channel. $\overline{BCD}$ is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For V.23 back channel mode, $\overline{BCD}$ turns on when either the MARK or SPACE frequency appears with sufficient level at the received carrier (RC) input.

For 202 back channel mode, $\overline{BCD}$ turns on in response to a 387Hz tone of sufficient level at the RC input. In this case $\overline{BCD}$ is equivalent to the signal, Secondary Received Line Signal Detector, for 202 S/T modems, or Supervisory Received Data for 202 C/D modems.

BACK TRANSMITTED DATA (BTD)

This line is equivalent to TRANSMITTED DATA for the main channel, except it belongs to the back channel. BTD is meaningful only when a 202 or V.23 mode is selected by MC_0-MC_4. For 202 back transmission of on/off keying, BTD should be fixed at a HIGH level.

BACK RECEIVED DATA (BRD)

This line is equivalent to RECEIVED DATA (except clamping) for the main channel, except it belongs to the back channel. BRD is meaningful only when a V.23 mode is selected by MC_0-MC_4. Under the following conditions this output is forced HIGH:

1. $\overline{BRD}$ HIGH
2. $\overline{DTR}$ HIGH
3. V.21/103 mode
4. During auto-answer
5. When $\overline{BRTS}$ ON and $\overline{RTS}$ OFF in V.23 modes only

TRANSMITTED CARRIER (TC)

This analog output is the modulated carrier to be conditioned and sent over the phone line.

RECEIVED CARRIER (RC)

This input is the analog signal received from the phone line. The modem extracts the information contained in this modulated carrier and converts it into a serial data stream for presentation at the RECEIVED DATA (BACK RECEIVED DATA) output.

$\overline{RING}$

This input signal permits auto-answer capability by responding to a ringing signal from a data access arrangement. If a ringing signal is detected ($\overline{RING}$ LOW) and $\overline{DTR}$ is LOW, the modem begins a sequence to generate an answer tone at the TC output.

$XTAL_1$, $XTAL_2$

Master timing of the modem is provided by either a crystal connected to these two inputs or an external clock inserted into $XTAL_1$. The value of the crystal or the external clock frequency must be 2.4576MHz ±.01%.

V_{CC}

+5 volt power supply. (±5%)

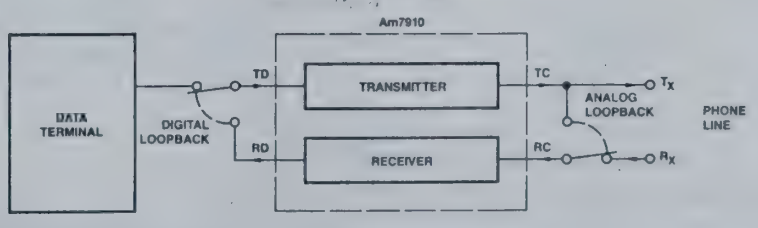
V_{BB}

−5 volt power supply. (±5%)

TABLE 1.

MC_4	MC_3	MC_2	MC_1	MC_0	
0	0	0	0	0	Bell 103 Originate 300bps full duplex
0	0	0	0	1	Bell 103 Answer 300bps full duplex
0	0	0	1	0	Bell 202 1200bps half duplex
0	0	0	1	1	Bell 202 with equalizer 1200bps half duplex
0	0	1	0	0	CCITT V.21 Orig 300bps full duplex
0	0	1	0	1	CCITT V.21 Ans 300bps full duplex
0	0	1	1	0	CCITT V.23 Mode 2 1200bps half duplex
0	0	1	1	1	CCITT V.23 Mode 2 with equalizer 1200bps half duplex
0	1	0	0	0	CCITT V.23 Mode 1 600bps half duplex
0	1	0	0	1	Reserved
0	1	0	1	0	
0	1	0	1	1	
0	1	1	0	0	
0	1	1	0	1	
0	1	1	1	0	
0	1	1	1	1	
1	0	0	0	0	Bell 103 Orig loopback
1	0	0	0	1	Bell 103 Ans loopback
1	0	0	1	0	Bell 202 Main loopback
1	0	0	1	1	Bell 202 with equalizer loopback
1	0	1	0	0	CCITT V.21 Orig loopback
1	0	1	0	1	CCITT V.21 Ans loopack
1	0	1	1	0	CCITT V.23 Mode 2 main loopback
1	0	1	1	1	CCITT V.23 Mode 2 with equalizer loopback
1	1	0	0	0	CCITT V.23 Mode 1 main loopback
1	1	0	0	1	CCITT V.23 Back loopback
1	1	0	1	0	Reserved
1	1	0	1	1	
1	1	1	0	0	
1	1	1	0	1	
1	1	1	1	0	
1	1	1	1	1	

Figure 3. Loopback Configurations



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DGND

Digital signal ground pin.

AGND

Analog signal ground pin (for TRANSMITTED CARRIER and RECEIVED CARRIER).

CAP_1, CAP_2

Connection points of external capacitor/resistor required for proper operation of on-chip analog-to-digital converter.

Recommended values are: C = 2000pF ±10%,
R = 100Ω ±10%.

$\overline{RESET}$

This input signal is for a reset circuit which operates in either of two modes. It automatically resets when power is applied to the device, or it can be activated by application of an external active low TTL pulse.

THEORY OF OPERATION

The Am7910 MODEM consists of three main sections, shown in the block diagram of Figure 2 – Transmitter, Receiver, and Interface Control.

TRANSMITTER (Modulator)

The transmitter, shown in Figure 4, receives binary digital data from a source such as a UART and converts the data to an analog signal using frequency shift keying (FSK) modulation. This analog signal is applied to the phone line through a DAA or acoustic coupler. FSK is a modulation technique which encodes one bit per baud. A logic one applied to the TRANSMITTED DATA (TD) input causes a sine wave at a given frequency to appear at the analog TRANSMITTED CARRIER (TC) output. A logic zero applied to input TD causes a sine wave of a different frequency to appear at the TC ouput. As the data at the TD input switches between logical one and zero, the TC output switches between the two frequencies. In the Am7910 this switching between frequencies is phase continuous. The frequencies themselves are digitally synthesized sine functions.

The frequencies for each modem configuration available in the Am7910 are listed in Table 3a.

The process of switching between two frequencies as in FSK generates energy at many more frequencies than the two used in the modulation. All the transmitted information can be recovered from a frequency band B Hz wide, where B is the bit rate or maximum rate of change of the digital data at the TD input. This band is centered about a frequency, f_C,

where $f_C = f_1 + (f_2 - f_1)/2$

(f_1 = lower of two FSK frequencies)

(f_2 = higher of two FSK frequencies)

In addition to this primary information band, there exist side bands containing redundant information. It is desirable to attenuate these bands for two reasons:

1. The phone companies have specifications on the amount of energy allowed in certain frequency bands on the line.
2. If two independent information channels are present simultaneously on the line (e.g. 300 bps full duplex or 1200 bps half duplex with back), the redundant transmitter components may fall in the frequency band of the local receiver channel and interfere with detection. In the Am7910 these redundant and undesirable components are attenuated by digital bandpass filters.

Following the digital bandpass filters, the filtered FSK signal is converted to an analog signal by an on-chip DAC operating at a high sample rate. This analog FSK signal is finally smoothed by a simple on-chip analog low pass filter.

RECEIVER (Demodulator)

A simplified block diagram of the Am7910 FSK receiver is shown in Figure 5. Data transmitted from a remote site modem over the phone line is an FSK-modulated analog carrier. This carrier is applied to the RECEIVED CARRIER (RC) pin via a DAA or acoustic coupler. The first stage of the demodulator is a simple on-chip analog low pass anti-alias filter. The output of this is converted into digital form and filtered by digital bandpass filters to improve the signal to noise ratio and reject other independent channel frequencies associated with the phone line in the case of full duplex configuration. The bandpass filtered output is digitally demodulated to recover the binary data. A carrier detect signal is also digitally extracted from the received line carrier to indicate valid data.

Figure 4. Transmitter Block Diagram

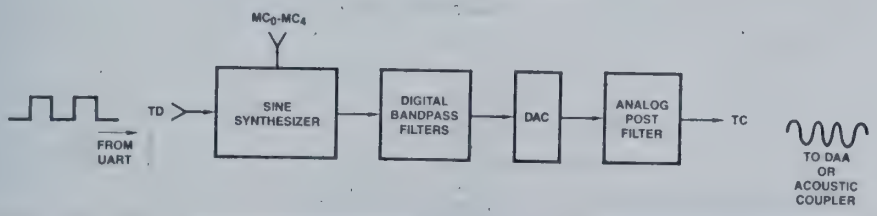

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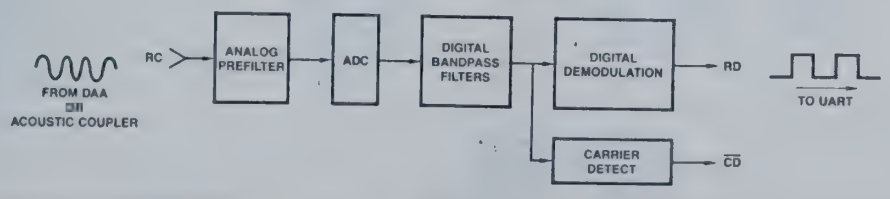
Figure 5. Receiver Block Diagram



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INTERFACE CONTROL

This section controls the handshaking between the modem and the local terminal. It consists primarily of delay generation counters, two state machines for controlling transmission and reception, and mode control decode logic for selecting proper transmit frequencies and transmit and receive filters according to the selected modem type. Inputs and outputs from this section are as follows:

$\overline{\text{REQUEST TO SEND}}$ (Main and Back)
$\overline{\text{CLEAR TO SEND}}$ (Main and Back)
$\overline{\text{CARRIER DETECT}}$ (Main and Back)
$\overline{\text{RING}}$
MC0-MC4
$\overline{\text{DATA TERMINAL READY}}$

Internal logic clamps protocol signals to different levels under certain conditions (e.g., initial conditions).

When Bell 103/113 and V.21 modem configurations are selected, the back channel signals are non-functional.

Figures 8 and 9 depict the sequencing of the two state machines. State machine 1 implements main or back channel transmission and the auto-answer sequence. State machine 2 implements reception on main or back channel.

The state machine powers on to the state labelled INITIAL CONDITIONS. Handshake signals are set to or assumed to be the levels listed in Table 2. The machine then waits for DATA $\overline{\text{TERMINAL READY}}$ (DTR) to be turned on. Whenever DTR is turned to the OFF state from an ON condition, each state machine and external signals return to the initial conditions within 25 microseconds. After DTR is turned ON the Am7910 becomes operational as a modem and the state machines proceed as depicted in the flowcharts.

The definitions of the terms Full Duplex and Half Duplex used in these flowcharts are depicted below (Figs. 6 and 7). "Full Duplex" applies to all 103/113, V.21 modes. "Half Duplex" applies to 202 and V.23, both forward and backward channel.

Full Duplex: Data can be transmitted and received simultaneously at a rate of 300 baud. Two independent 300Hz channels are frequency multiplexed into the 3000Hz bandwidth of the phone line. The Am7910 configurations for the Bell 103/113 and CCITT V.21 can be operated full duplex.

Half Duplex: In half duplex with back channel, the modem may transmit at 1200/600 baud and receive at 5/75 baud. Alternatively it may transmit at 5/75 baud and receive at 1200/600 baud. Examples are Bell 202 and CCITT V.23.

TABLE 2.
INITIAL CONDITIONS

Data Terminal Ready ($\overline{\text{DTR}}$)	OFF
Request to Send ($\overline{\text{RTS}}$)	OFF
Clear to Send ($\overline{\text{CTS}}$)	OFF
Transmitted Data (TD)	Ignored
Back Channel Request to Send ($\overline{\text{BRTS}}$)	OFF
Back Channel Clear to Send ($\overline{\text{BCTS}}$)	OFF
Back Channel Transmitted Data (BTD)	Ignored
Ring ($\overline{\text{RING}}$)	OFF
Carrier Detect ($\overline{\text{CD}}$)	OFF
Received Data (RD)	MARK
Back Channel Carrier Detect ($\overline{\text{BCD}}$)	OFF
Back Channel Received Data (BRD)	MARK

Figure 6. Full Duplex

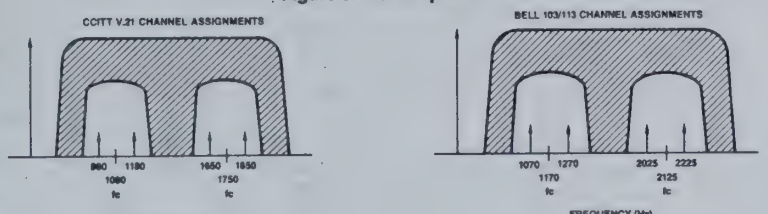

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Figure 7. Half Duplex

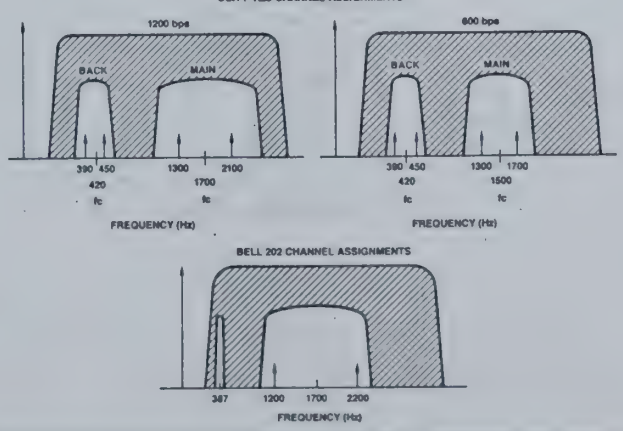

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TABLE 3(a). FREQUENCY PARAMETERS

Modem	Baud Rate (BPS)	Duplex	Transmit Frequency		Receive Frequency		Answer Tone Freq Hz
			Space Hz	Mark Hz	Space Hz	Mark Hz	
Bell 103 Orig	300	Full	1070	1270	2025	2225	–
Bell 103 Ans	300	Full	2025	2225	1070	1270	2225
CCITT V.21 Orig	300	Full	1180	980	1850	1650	–
CCITT V.21 Ans	300	Full	1850	1650	1180	980	2100
CCITT V.23 Mode 1	600	Half	1700	1300	1700	1300	2100
CCITT V.23 Mode 2	1200	Half	2100	1300	2100	1300	2100
CCITT V.23 Mode 2 Equalized	1200	Half	2100	1300	2100	1300	2100
Bell 202	1200	Half	2200	1200	2200	1200	2025
Bell 202 Equalized	1200	Half	2200	1200	2200	1200	2025
CCITT V.23 Back	75	–	450	390	450	390	–
Bell 202 Back	5	–	•	•	••	••	–

*($\overline{BRTS}$ LOW) and (BTD HIGH): 387Hz at TC **387Hz at RC: $\overline{BCD}$ LOW
*($\overline{BRTS}$ HIGH) or (BTD LOW): 0 volts at TC **No 387Hz at RC: $\overline{BCD}$ HIGH
*Meets new CCITT R20 frequency tolerance.

Frequency tolerance is less than ±0.4Hz with 2.4576MHz Crystal. Except Bell 202 which is +1Hz (1200 Hz, mark)

TABLE 3(b). TIMING PARAMETERS (Refer to Figures 10, 11 and 12 for Timing Diagrams)

Symbol	Description	Bell 103 Orig	Bell 103 Ans	CCITT V.21 Orig	CCITT V.21 Ans	CCITT V.23 Mode 1	CCITT V.23 Mode 2	CCITT V.23 Mode 2 EQ	Bell 202	Bell 202 EQ	CCITT V.23 Back	Bell 202 Back	Units
$t_{RC(On)}$	Request-to-Send to Clear-to-Send ON Delay	208.3	208.3	400	400	208.3	208.3	208.3	183.3	183.3	–	–	msec ±0.3%
$t_{RC(Off)}$	Request-to-Send to Clear-to-Send OFF Delay	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5	–	–	msec ±0.25%
$t_{BRC(On)}$	Back Channel Request-to-Send to Clear-to-Send ON Delay	–	–	–	–	–	–	–	–	–	82.3	–	msec ±0.64%
$t_{BRC(Off)}$	Back Channel Request-to-Send to Clear-to-Send OFF Delay	–	–	–	–	–	–	–	–	–	0.5	–	msec ±25%
$t_{CD(On)}$	Carrier Detect ON Delay	94-106	94-106	301-312	301-312	11.4-15.4	11.4-15.4	11.4-15.4	18-22	18-22	–	–	msec
$t_{CD(Off)}$	Carrier Detect OFF Delay	21-40	21-40	21-40	21-40	5.4-13.3	5.4-13.3	5.4-13.3	12.4-23.4	12.4-23.4			msec
$t_{BCD(On)}$	Back Channel Carrier Detect ON Delay	–	–	–	–	–	–	–	–	–	17-25	17-25	msec
$t_{BCD(Off)}$	Back Channel Carrier Detect OFF Delay	–	–	–	–	–	–	–	–	–	21-38	21-38	msec
t_{AT}	Answer Tone Duration	–	1.9	–	3.0	3.0	3.0	3.0	1.9	1.9	–	–	sec ±0.44%
t_{SIL}	Silence Interval before Transmission	1.3	1.3	1.9	1.9	1.9	1.9	1.9	1.3	1.3	–	–	sec ±0.64%
t_{SQ}	Receiver Squelch Duration	–	–	–	–	156.3	156.3	156.3	156.3	156.3	–	–	msec ±3.3%
t_{STO}	Transmitter Soft Turn-Off Duration	–	–	–	–	–	–	–	24	24	–	–	msec ±2.3%
t_{RI}	Minimum $\overline{RI}$ Low Duration	–	25	–	25	25	25	25	25	25	–	–	μs

CALL ESTABLISHMENT

Before two modems can exchange data, an electrical connection through the phone system must be established. Although it may assist in call establishment, a modem typically does not play a major role. A call may be originated manually or automatically and it may be answered manually or automatically.

Manual Calling – Manual calling is performed by a person who dials the number, waits for an answer , then places the calling modem into data transmission mode.

Automatic Calling – Automatic calling is typically performed by an automatic calling unit (ACU) which generates the appropriate dialing pulse or dual-tone sequence required to call the remote (called) modem. The ACU also has the ability to detect an answer tone from the called modem and place the calling modem into data transmission mode.

Manual Answering – Manual answering is performed by a person who hears the phone ring, lifts the receiver, causes the called modem to send an answer tone to the calling modem, and places the called modem into data transmission mode.

Automatic Answering – Automatic answering is performed by a called modem with a data access arrangement (DAA). The DAA detects a ringing signal, takes the phone circuit off-hook (corresponding to lifting the receiver) and instructs the called modem to commence the auto-answer sequence. Next the called modem sends out silence on the line, followed by an answer tone. When this tone is detected by the calling modem, the connection is considered to have been established.

The Am7910 provides assistance for automatic answering through the $\overline{\text{RING}}$ signal as follows. Observe the upper right-hand portion of Figure 8(a). Assume that $\overline{\text{DATA TERMINAL READY}}$ ($\overline{\text{DTR}}$) has recently been asserted to cause exit from the initial conditions. Note that if $\overline{\text{DTR}}$ remains OFF, $\overline{\text{RING}}$ is ignored. Assume also that $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are OFF and that the mode control lines (MC0-MC4) select a normal modem configuration, not a loopback mode. Automatic answering is initiated by receipt of a LOW level at the $\overline{\text{RING}}$ input, causing entrance to the auto-answer sequence depicted in Figure 8(c).

The Am7910 outputs silence (0.0 volts) at its TRANSMITTED CARRIER (TC) output for a time, t_{SIL}, followed by the answer tone for a time, t_{AT}. The $\overline{\text{CARRIER DETECT}}$ ($\overline{\text{CD}}$) pin is clamped OFF and the RECEIVED DATA (RD) signal is therefore clamped to a MARK (HIGH) during the auto-answer sequence. Upon completion of the answer tone, $\overline{\text{CD}}$ is released. If the mode lines (MC0-MC4) select a 202 or V.23 mode, the transmit filters are set to the forward channel and the receive filters are set to the back channel during the auto answer sequence.

At the end of the auto-answer sequence, return is made to point A in the loop at the upper right-hand portion of Figure 8(a). Note that since the answer flag has been set, the auto-answer sequence cannot be entered again unless $\overline{\text{DTR}}$ is first turned OFF, then ON. At this point the phone line connection has been established and data transmission or reception may begin.

The $\overline{\text{RING}}$ input may be activated from a conditioned DAA Ring Indicator output for automatic answering or it may be activated by a switch for manual answering. Tying $\overline{\text{RING}}$ HIGH will disable the auto-answer function of the Am7910.

DATA TRANSMISSION

Full Duplex

Following call establishment, full duplex data transmission can be started by either the called or calling modem. In other words, if the connection has been established and the modem is looping through point A in Figure 8(a), it no longer matters which is the called and which is the calling modem. Data transmission is initiated by asserting $\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$). At this time the TRANSMITTED DATA (TD) input will be released and a modulated carrier can appear at the TRANSMITTED CARRIER (TC) output. Following a delay, t_{RCON}, $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) will turn ON. At this time, data may be transmitted through the TD input. It is a common protocol for the user to always present a MARK at the TD input before $\overline{\text{RTS}}$ is asserted and during the t_{RCON} delay.

Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. Following a short delay, t_{RCOFF}, $\overline{\text{CTS}}$ turns OFF. As soon as $\overline{\text{RTS}}$ goes OFF, the TD input is ignored and the TC output is set to 0.0 volts (silence). After $\overline{\text{CTS}}$ turns OFF, the state machine returns to point A in Figure 8(a).

Half Duplex

When a half duplex mode is selected (202 or V.23), data transmission can be either on the main channel at 1200/600 baud or on the back channel at 5/75 baud. In normal half duplex operation a single modem is either transmitting on the main and receiving on the back channel or vice versa. In the Am7910 control of the transmitter and receiver filters to the proper channel is performed by $\overline{\text{RTS}}$. When $\overline{\text{RTS}}$ is asserted, the transmitter filters and synthesizer are set to transmit on the main channel; the receiver filters are set to receive on the back channel. Therefore, whenever $\overline{\text{RTS}}$ is on, $\overline{\text{BRTS}}$ should not be asserted since the transmitter cannot be used for the back channel. When $\overline{\text{RTS}}$ is OFF and a half duplex mode is selected, the transmitter filters and synthesizer are set to the back channel; the receiver filters are set to the main channel. If $\overline{\text{RTS}}$ and $\overline{\text{BRTS}}$ are asserted simultaneously, $\overline{\text{RTS}}$ will take precedence. However, if $\overline{\text{BRTS}}$ is asserted before $\overline{\text{RTS}}$ and the back channel data transmission sequence has been entered (Figure 8(b)), $\overline{\text{RTS}}$ will be ignored until $\overline{\text{BRTS}}$ is turned OFF.

The state machine sequences for main and back channel transmission differ slightly and are depicted in Figure 8. Assume the state machine is idling through point A in Figure 8(a).

Main Channel

This transmission sequence is entered if a 202 or V.23 mode is selected and $\overline{\text{RTS}}$ is asserted. Since the receiver is now forced to the back channel, the RECEIVED DATA (RD) signal is clamped to a MARK; and the $\overline{\text{CARRIER DETECT}}$ signal is clamped OFF. The TRANSMITTED DATA input (TD) is released and a carrier appears at the TRANSMITTED CARRIER output which follows the MARK/SPACE applied to TD. $\overline{\text{RTS}}$ turning ON initiates a delay, t_{RCON}, at the end of which the $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) output goes LOW. When $\overline{\text{CTS}}$ goes LOW data may be transmitted through input TD. Data transmission continues until $\overline{\text{RTS}}$ is turned OFF. At this time several events are initiated. First a delay, t_{RCOFF}, is initiated at the end of which $\overline{\text{CTS}}$ turns OFF. The TD input is ignored as soon as $\overline{\text{RTS}}$ goes OFF. If a 202 mode is selected, a soft turn-off tone appears at the TC output for a time, t_{STO}, followed by silence (0.0 volts). For both 202 and V.23 modes a squelch period, t_{SQ}, is initiated when $\overline{\text{RTS}}$ goes OFF. During this period the $\overline{\text{CD}}$ output is clamped OFF, forcing the RD output to a MARK condition. The squelch period begins as soon as $\overline{\text{RTS}}$ goes OFF and thus overlaps both t_{RCOFF} and t_{STO}. At the end of the squelch period, the state machine returns to the idle loop at point A in Figure 8(a).

The reasons for squelch and soft-turnoff are as follows:

Soft Turn-Off: When $\overline{\text{RTS}}$ is turned OFF at the end of a message, transients occur which may cause spurious space signals to be received at a remote modem. During soft turn-off the modem transmits a soft carrier frequency for a period, t_{STO}, after $\overline{\text{RTS}}$ is

turned OFF. This resu
DATA (RD) line of the

Squelch: The local re
OFF, until the start of c
demodulated. The pro
turned OFF is called s

Back Channel

This transmission sequ
202 or V.23 mode is sel
The $\overline{\text{BACK CARRIER}}$ [
the BACK RECEIVED
MARK. The BACK TF
leased and a carrier ap
MARK/SPACE applied
delay, t_{BRCON}, at the e
($\overline{\text{BCTS}}$) output goes LC
transmitted through inp
$\overline{\text{BRTS}}$ is turned OFF. T
the TC output is silen
delay, t_{BRCOFF}, the ou
and BRD are released
point A of Figure 8(a).

In 202 back channel r
$\overline{\text{BRTS}}$ controls the ON
LOW, 387Hz appears
volts appears at TC.

DATA RECEPTION

Data reception is contr
Figure 9. At power on t
remains there until $\overline{\text{DT}}$
$\overline{\text{CARRIER DETECT}}$($\overline{\text{CD}}$
occurs.

Full Duplex

In full duplex data rece
at any time after the pl
Reception is independ
detects a valid carrier fo
turned ON, the RECEI
valid data can be obta
receiver detects loss of
time the $\overline{\text{CD}}$ output is tur
The state machine retu

turned OFF. This results in a steady MARK on the RECEIVED DATA (RD) line of the remote modem.

Squelch: The local receiver must be turned OFF after $\overline{RTS}$ is OFF, until the start of carrier detect, so that line transients are not demodulated. The process of disabling the receiver after $\overline{RTS}$ is turned OFF is called squelching.

Back Channel

This transmission sequence, shown in Figure 8(b), is entered if a 202 or V.23 mode is selected, $\overline{RTS}$ is OFF, and $\overline{BRTS}$ is asserted. The $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) output is forced OFF and the BACK RECEIVED DATA (BRD) output is clamped to a MARK. The BACK TRANSMITTED DATA input (BTD) is released and a carrier appears at the TC output which follows the MARK/SPACE applied to BTD. Turning ON $\overline{BRTS}$ initiates a delay, t_{BRCON}, at the end of which the $\overline{BACK\ CLEAR\ TO\ SEND}$ ($\overline{BCTS}$) output goes LOW. When $\overline{BCTS}$ goes LOW data may be transmitted through input BTD. Data transmission continues until $\overline{BRTS}$ is turned OFF. The input BTD is immediately ignored and the TC output is silenced (set to 0.0 volts). Following a short delay, t_{BRCOFF}, the output $\overline{BCTS}$ goes OFF. The signals $\overline{BCD}$ and BRD are released and the state machine returns to idle at point A of Figure 8(a).

In 202 back channel mode, BTD should be tied HIGH. Then $\overline{BRTS}$ controls the ON/OFF keying modulation. When $\overline{BRTS}$ is LOW, 387Hz appears at the TC output; when $\overline{BRTS}$ is HIGH, 0 volts appears at TC.

DATA RECEPTION

Data reception is controlled by state machine 2 and depicted in Figure 9. At power on the machine enters initial conditions and remains there until $\overline{DTR}$ is asserted. It then loops until either $\overline{CARRIER\ DETECT}$($\overline{CD}$) or $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) occurs.

Full Duplex

In full duplex data reception, $\overline{CARRIER\ DETECT}$ may appear at any time after the phone connection has been established. Reception is independent of transmission. When the receiver detects a valid carrier for at least a time, t_{CDON}, the output $\overline{CD}$ is turned ON, the RECEIVED DATA (RD) output is released, and valid data can be obtained at RD. Data is received until the receiver detects loss of carrier for at least a time, t_{CDOFF}. At this time the $\overline{CD}$ output is turned OFF and RD is clamped to a MARK. The state machine returns to the idle loop at point E.

Half Duplex

As discussed in the data transmission section above, when a half duplex mode has been selected, the signal $\overline{RTS}$ controls whether the main channel is transmitting or receiving. The back channel can only do the opposite from the main. If $\overline{RTS}$ is OFF, then $\overline{CARRIER\ DETECT}$ may be asserted and the data reception sequence is identical to that discussed above for full duplex reception. As long as $\overline{RTS}$ remains OFF, $\overline{BACK\ CARRIER\ DETECT}$ will never be asserted. If $\overline{RTS}$ is ON, then $\overline{CARRIER\ DETECT}$ will never be asserted. Instead the receiver will look for a valid carrier in the back channel frequency band. If a valid carrier exists for at least a time, t_{BCDON}, the output $\overline{BACK\ CARRIER\ DETECT}$ ($\overline{BCD}$) is turned ON, the BACK RECEIVED DATA (BRD) output is released and valid data can be obtained at BRD. Data is received until the receiver detects loss of back channel received signal for at least time, t_{BCDOFF}. At this time the $\overline{BCD}$ output is turned OFF. Data output, BRD, is clamped to a MARK if a V.23 mode is selected. For 202 back channel mode, $\overline{BCD}$ represents the received data. The BRD output can be ignored. The state machine returns to the idle loop at point E.

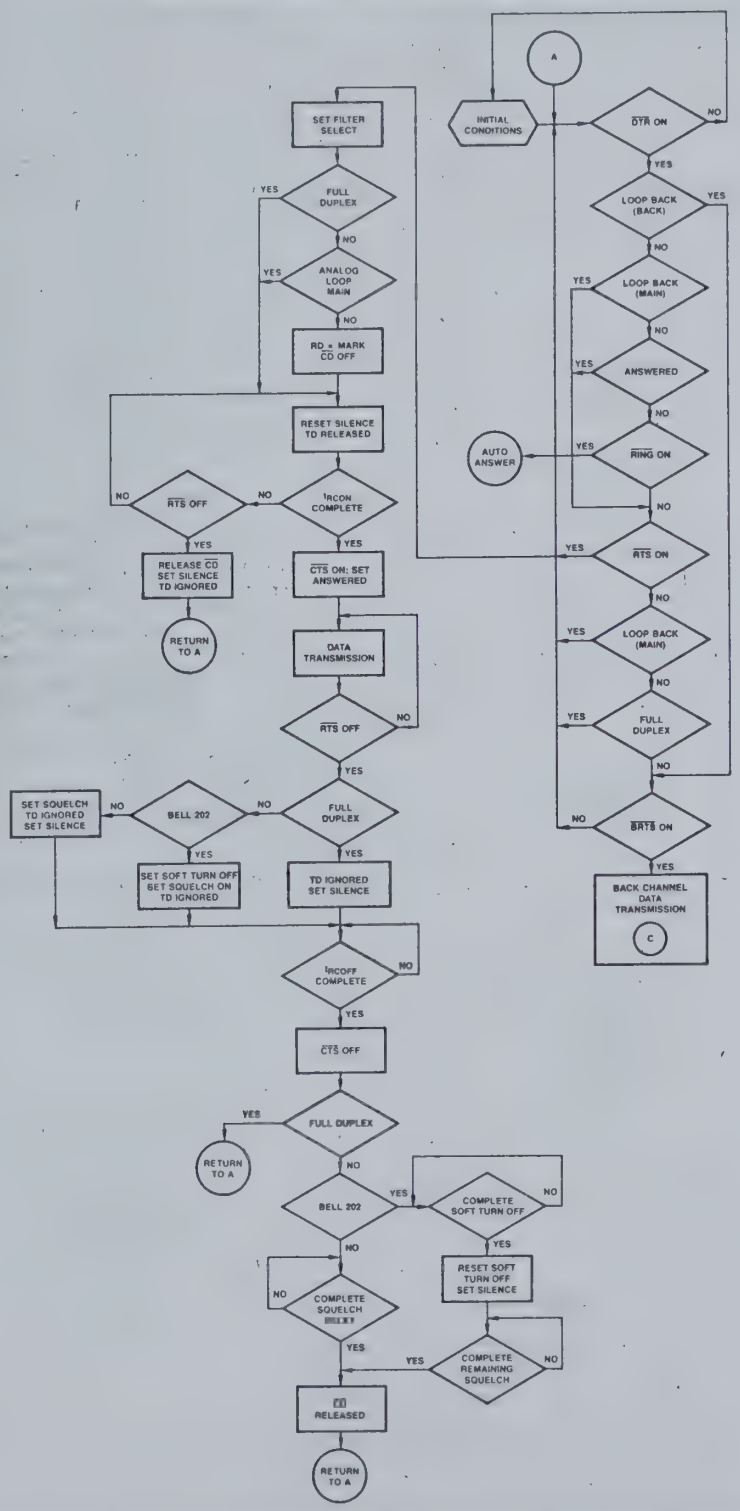
LOOPBACK

Ten modes exist to allow both analog and digital loopback for each modem specification met by the Am7910. When a loopback mode is selected, the signal processing (filters, etc.) for both the transmitter and receiver is set to process the same channel or frequency band. This allows the analog output, TRANSMITTED CARRIER, and the analog input, RECEIVED CARRIER, to be connected for local analog loopback. Alternatively the digital data signals, TD and RD or BTD and BRD, can be connected externally, allowing a remote modem to test the local modem with its digital data signals looped back.

When a loopback mode is selected, the state machine sequences are altered slightly. First, auto-answer is disabled. Second, if a half duplex loopback mode is selected (202 or V.23), the local $\overline{CARRIER\ DETECT}$/$\overline{BCD}$ is not forced OFF when $\overline{RTS}$/$\overline{BRTS}$ is asserted.

The 202 and V.23 main loopback modes allow use in a 4-wire configuration at 1200 bps.

Figure 8(a). Transmit Main Channel State Diagram



0123BC4

Figure 8(b). Transmit

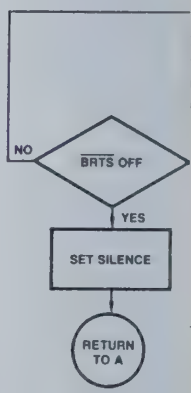


Figure 8(b). Transmit Back Channel State Diagram

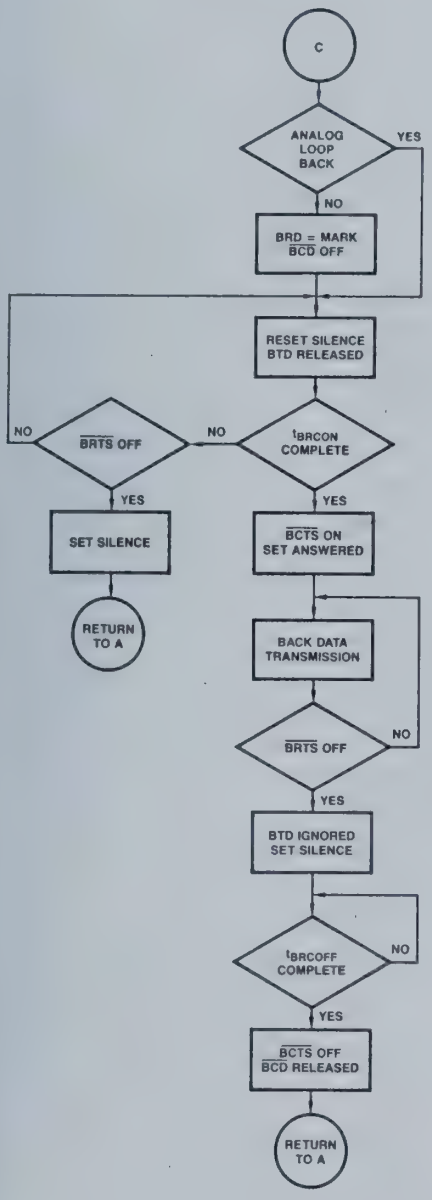


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Figure 8(c). Auto Answer State Diagram

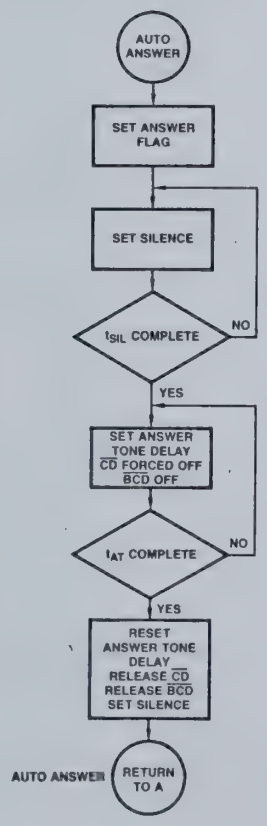

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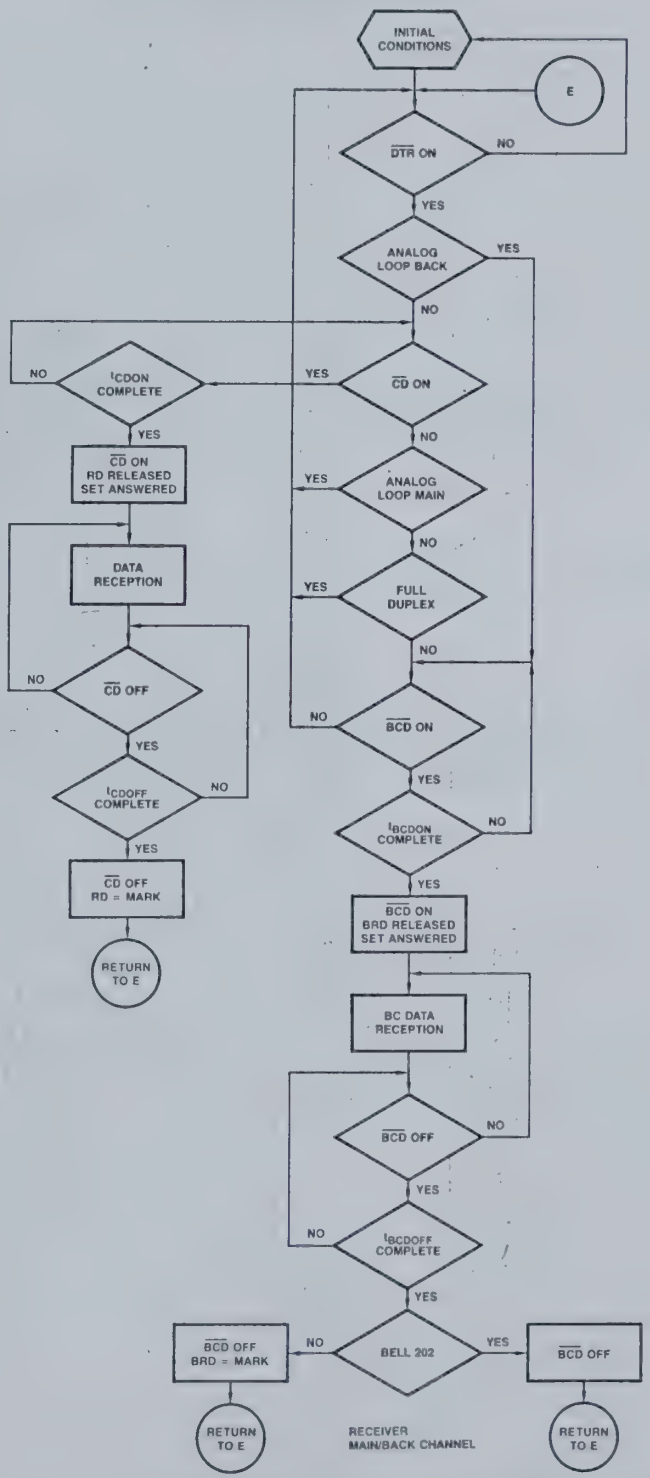
Figure 9. Receiver Main/Back Channel State Diagram



01238C-11

Figure 10. BELL 202 Handshake Timing

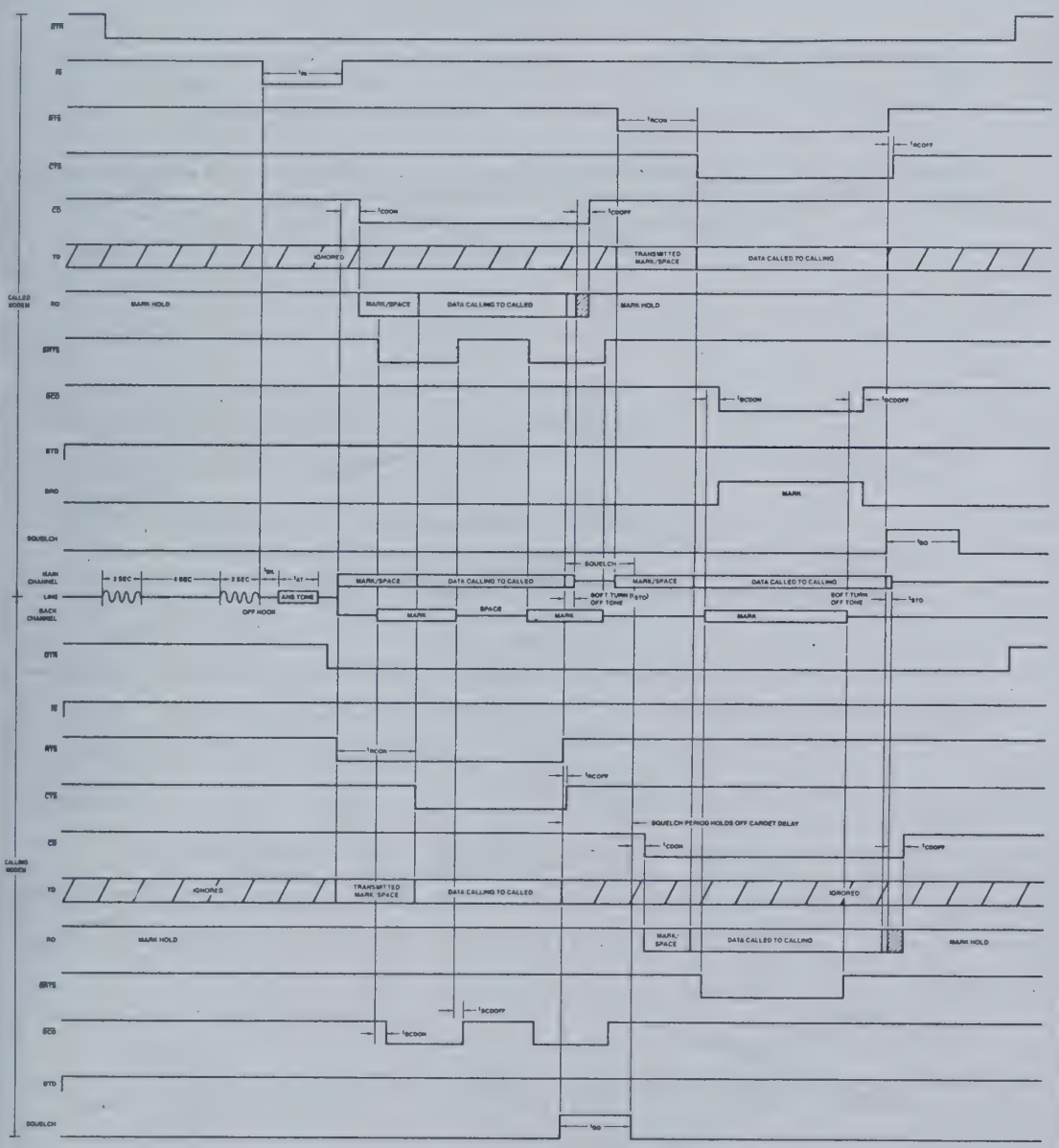


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Figure 11. CCITT V.23 Handshake Timing

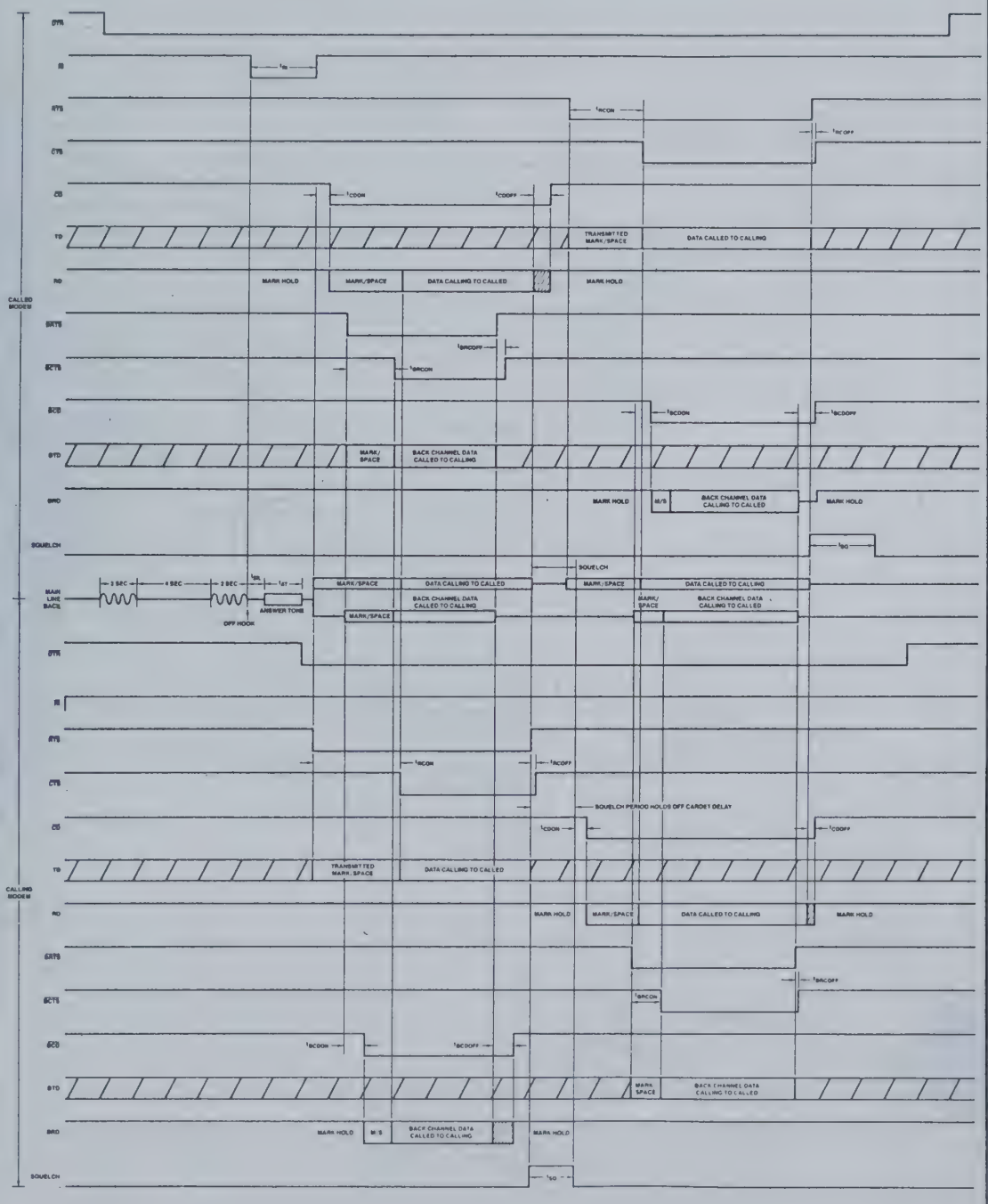

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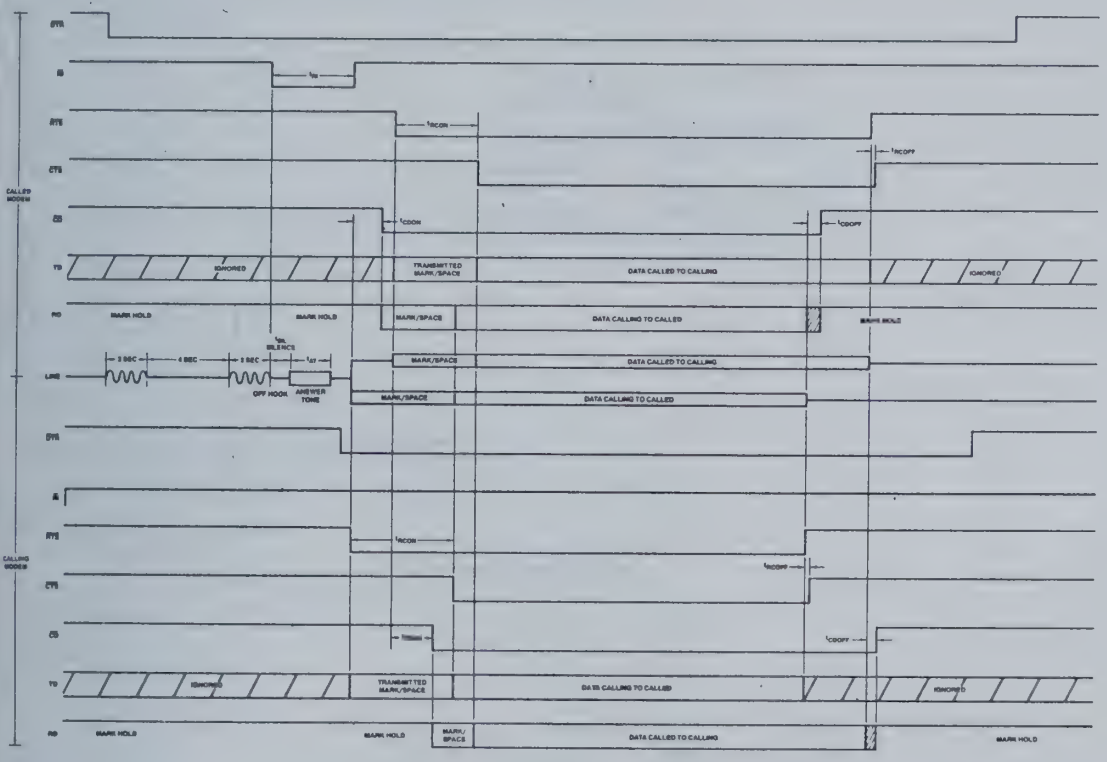
Figure 12. BELL 103/CCITT V.21 Handshake Timing



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CLOCK GENERATION

Master timing of the modem is provided by either a crystal connected to the $XTAL_1$ and $XTAL_2$ inputs or an external clock applied to the $XTAL_1$ input.

Crystal

When a crystal is used it should be connected as shown in Figure 13. The crystal should be a parallel resonance type, and its value must be 2.4576MHz ±.01%. A list of crystal suppliers is shown below.

External Clock

This clock signal could be derived from one of several crystal-driven baud rate generators. It should be connected to the $XTAL_1$ input and the $XTAL_2$ input must be left floating. The timing parameters required of this clock are shown in Figure 13 and the values are listed in Table 4.

Figure 13. Clock Generation

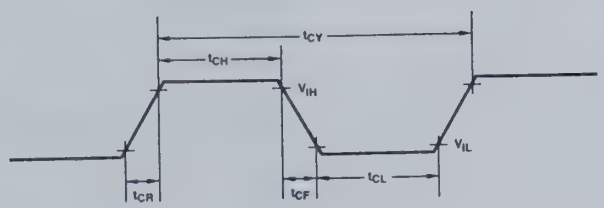
Crystal Information (f_C = 2.4576MHz)

Manufacturer	P/N	C_1	C_2
M-Tron	MP-2	20pF	20pF
Monitor Products	MM-33	20pF	20pF

Note: Rise time of V_{CC} must be greater than 5msec to insure proper crystal oscillator start-up.

*Capacitors values vary with different crystal manufacturers.

(a)



(b)

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TABLE 4.
CLOCK PARAMETERS

Symbol	Parameters	Min	Typ	Max	Units
t_{CY}	Clock Period	406.86	406.9	406.94	ns
t_{CH}	Clock High Time	165			ns
t_{CL}	Clock Low Time	165			ns
t_{CR}	Clock Rise Time			20	ns
t_{CF}	Clock Fall Time			20	ns

PRELIMINARY

POWER ON RESET

The reset circuit ope

Automatic Reset

In this mode an int
tered when power i
one capacitor must
14. Values shown v
supply (V_{CC}) rise ti
time constant.

External Reset

In this mode the de
by application of ar
input. The reset mu
reached at least 3.5

one of several crystal-
be connected to the
st be left floating. The
are shown in Figure 13

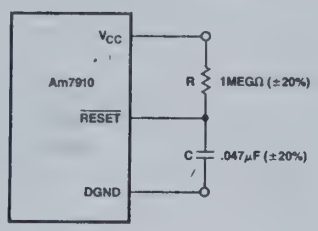
POWER ON RESET

The reset circuit operates in either of two modes.

Automatic Reset

In this mode an internal reset sequence is automatically entered when power is applied to the device. One resistor and one capacitor must be connected externally as shown in Figure 14. Values shown will work with most power supplies. Power supply (V_{CC}) rise time should be less than one half the RC time constant.

Figure 14. Automatic Reset



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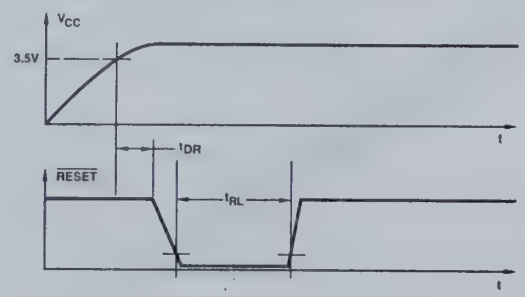
External Reset

In this mode the device may be forced into the reset sequence by application of an active LOW pulse applied to the $\overline{RESET}$ input. The reset must not be applied until the V_{CC} supply has reached at least 3.5V. Timing is diagrammed in Figure 15.

Figure 15. External Reset

TIMING DIAGRAMS



t_{DR} = delay from the time V_{CC} reaches 3.5V and the falling edge of $\overline{RESET}$ signal (>1μs)
t_{RL} = $\overline{RESET}$ LOW duration time (>t_{MCK} = 406ns)

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9

NOMINAL PERFORMANCE SPECIFICATIONS
TRANSMITTER (All Modem Types)

Input Data Format: Serial, asynchronous, standard TTL levels
Modulation Technique:
Binary, phase-coherent Frequency Shift Keying (FSK)
TC Output Level: −3dBm into 600Ω
Frequency Accuracy:
±0.4Hz all modems except Bell 202 (mark)
+1.0Hz Bell 202 (mark)
Harmonics: −45dB from fundamental for single tones

Delay uncertainty for TD logic input change to TC frequency change: ≤8.3μs

Out-of-band energy: See Figure 16

RECEIVER

Output Data Format: Serial, asynchronous, TTL levels
Demodulation Technique: Differential FM Detection
Sensitivity at Receiver Input: 0dBm to −48dBm
Frequency Deviation Tolerance: ±16Hz
Carrier Detect Threshold:

ON	>−43dBm ±1dB
OFF	<−48dBm ±1dB

TEST MEASUREMENT SETUP

Am7910 performance is characterized using the test equipment setup shown in Figure 17. The HP1645A data error analyzer is used to generate 511-bit pseudo random binary sequences (PRBS) at D_{OUT} for testing the modem. The 1645A also receives and analyzes the 511-bit digital pattern at D_{IN} after it has progressed around the test loop. A reference transmitter converts the digital sequence generated by the HP1645A into an FSK signal. The FSK signal is typically adjusted to different levels from −12 to −45dBm. The level-adjusted FSK signal or incident signal then passes through three pieces of equipment which comprise the telephone line simulator. The Wandel and Golterman TLN-1 and DLZ-4 simulate amplitude and group delay characteristics typical of a wide variety of phone lines. Line perturbations, such as amplitude hits and phase hits, may be injected by the Bradley 2A/2B.

The summing amplifier which drives the modem under test has three inputs. One of these inputs is the incident FSK signal which has been passed through a simulated phone line. The second input is from an optionally filtered noise source in order to simulate noise conditions which may be encountered on phone lines. The third input is from the transmitter of the Am7910 under test. This third input simulates the adjacent channel signal seen at the input of the Am7910 receiver due to the duplexer used on 2-wire lines. If 4-wire testing is being performed, the adjacent channel would not normally be included.

The HP3551A or HP3552A Transmission Test Set is used for measuring various levels which the modem under test is to receive. The levels of each of the three inputs to the summing amplifier should be measured independently of the other two inputs. For instance, the incident signal level should be measured by the transmission test set with no adjacent channel or noise present. The dashed line from the noise generator shows that the noise may or may not be measured at the output of the noise generator, depending on whether or not an optional filter is used, or on the characteristics of the filter.

Figure 16. Out-of-Band Transmitter Energy

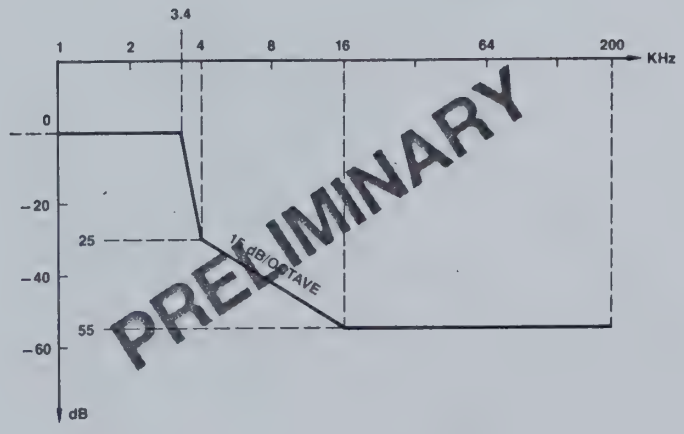

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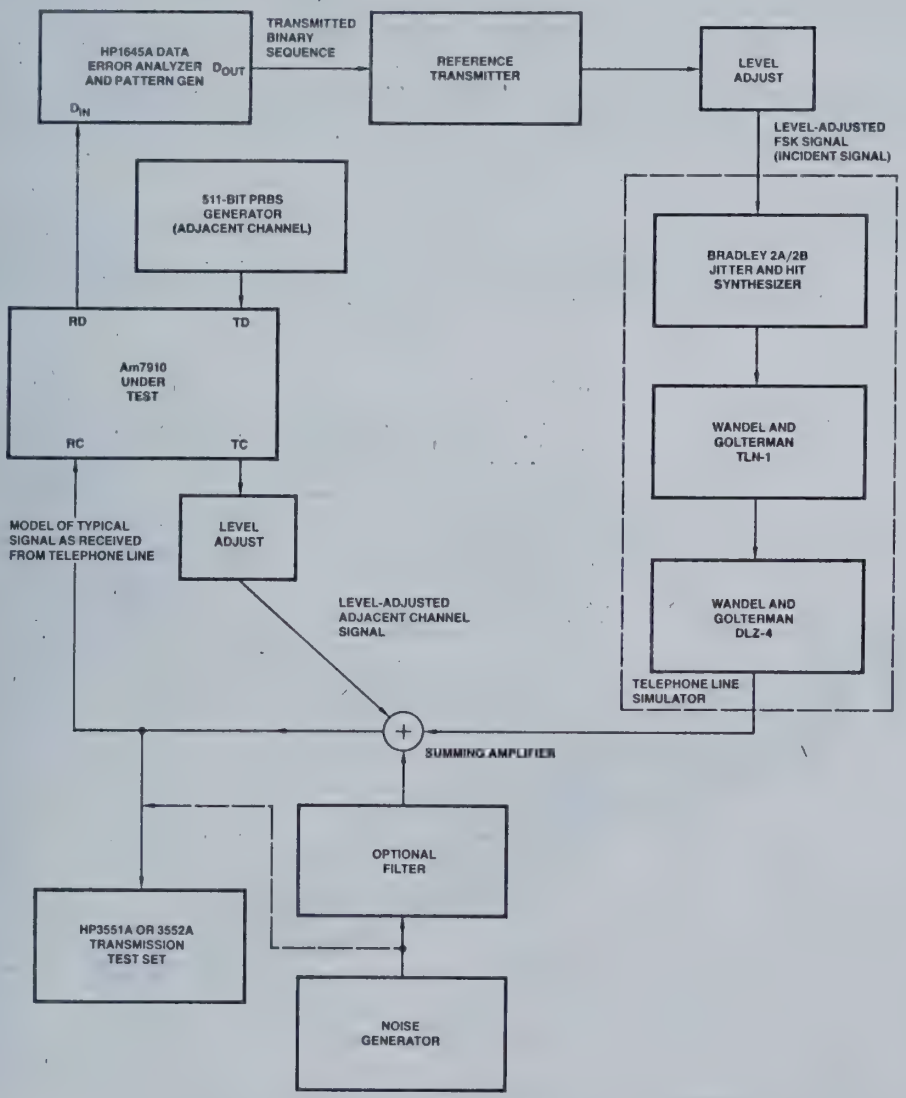
Figure 17. BER and Distortion Measurement Test Setup



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Am7910
MAXIMUM RATINGS

Storage Temperature	−65 to +125°C
Ambient Temperature under Bias	0 to +70°C
V_{CC} with Respect to V_{DGND}	+6V/−.4V
V_{BB} with Respect to V_{DGND}	−6V/+.4V
All Signal Voltages with Respect to V_{DGND}	±5V

The products described by this specification include internal circuitry designed to protect input devices from damaging accumulations of charge. It is suggested, nevertheless, that conventional precautions be observed during storage, handling and use in order to avoid exposure to excessive voltages.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING RANGE

Ambient Temperature	V_{CC}	V_{BB}	V_{AGND}	V_{DGND}
$0°C \leq T_A \leq +70°C$	+5.0V ±5%	−5.0V ±5%	0V ±50mV	0V

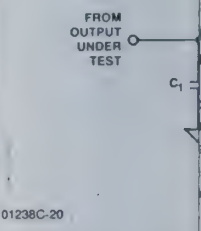
DC CHARACTERISTICS

Digital Inputs: TD, $\overline{RTS}$, MC_0–MC_4, $\overline{DTR}$, $\overline{RING}$, BTD, $\overline{BRTS}$
Digital Outputs: RD, $\overline{CTS}$, $\overline{CD}$, BRD, $\overline{BCTS}$, $\overline{BCD}$

Parameters	Description	Test Conditions	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -50\mu A$, $C_{LD} = 50pF$	2.4			Volts
V_{OL}	Output LOW Voltage	$I_{OL} = +2mA$, $C_{LD} = 50pF$			0.4	Volts
V_{IH}	Input HIGH Voltage		2.0		V_{CC}	Volts
V_{IL}	Input LOW Voltage		−0.5		+0.8	Volts
V_{IHC}	External Clock Input HIGH ($XTAL_1$)		3.8		V_{CC}	Volts
V_{ILC}	External Clock Input LOW ($XTAL_1$)		−0.5		0.8	Volts
V_{IHR}	External Reset Input HIGH ($\overline{RESET}$)		3.5		V_{CC}	Volts
V_{ILR}	External Reset Input LOW ($\overline{RESET}$)		−0.5		0.8	Volts
I_{IL}	Digital Input Leakage Current	$0 \leq V_{IN} \leq V_{CC}$	−10		+10	μA
I_{CC}	V_{CC} Supply Current				125	mA
I_{BB}	V_{BB} Supply Current				25	mA
C_{OUT}	Output Capacitance	$f_C = 1.0MHz$		5	15	pF
C_{IN}	Input Capacitance	$f_C = 1.0MHz$		5	15	pF
Analog Input (RC):						
R_{IN}	Input Resistance	$-1.6V < V_{RC} < +1.6V$	50			Kohms
V_{RC}	Operating Input Signal		−1.6		+1.6	Volts
V_{RCOS}	Allowed DC Input Offset	REF V_{AGND}	−30		+30	mV
Analog Output (TC):						
V_{TC}	Output Voltage	$R_L = 600\Omega$	−1.1		+1.1	Volts
V_{TCOS}	Output DC Offset			±200		mV

PRELIMINARY

STANDARD LOAD C



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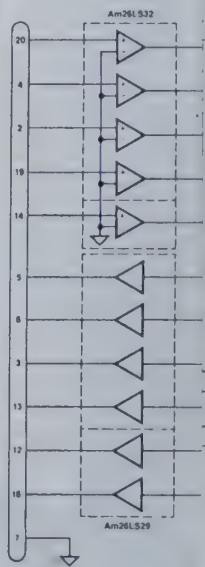
APPLICATIONS

Figure 18 depicts a s
amp and three resisto
transmitter output ont
nel data from the line.
cess Arrangement (D
ters. The TTL handsh
RS-232, RS-422, or
control lines are hardw



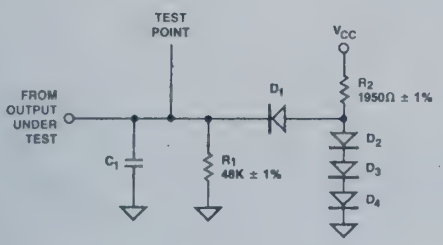
	+65 to +125°C
	0 to +70°C
	+6V/−.4V
	−6V/+.4V
	±5V

aging accumulations of
d use in order to avoid

. This is a stress rating
rational sections of this
vice reliability.

Max	Unit
	Volts
0.4	Volts
V_{CC}	Volts
+0.8	Volts
V_{CC}	Volts
	Volts
V_{CC}	Volts
0.8	Volts
+10	μA
125	mA
25	mA
15	pF
15	pF
	Kohms
+1.6	Volts
+30	mV
+1.1	Volts
	mV

STANDARD LOAD CIRCUIT



Notes: 1. C_1 = 50pF including stray and wiring capacitance
2. All diodes are IN3064 or equivalent
3. All resistors are 1/8 watt
4. V_{CC} = 5 volts ±1%

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APPLICATIONS

Figure 18 depicts a stand-alone Am7910 configuration. An op amp and three resistors provide a duplexor function to put the transmitter output onto the line while receiving adjacent channel data from the line. Connection to the line is via a Data Access Arrangement (DAA). Note the lack of external analog filters. The TTL handshake signals may be level converted to RS-232, RS-422, or V.24 using appropriate devices. Mode control lines are hardwired or connected to switches.

Figure 19 depicts use of the Am7910 when a microprocessor resides in the same physical location. The duplexor/line interface is identical to the above configuration. However, the handshake signals interface directly to a UART-type device which in turn interfaces to a microprocessor. The mode control lines might also be controlled by the microprocessor.

Figure 18. Stand-Alone Am7910 Application

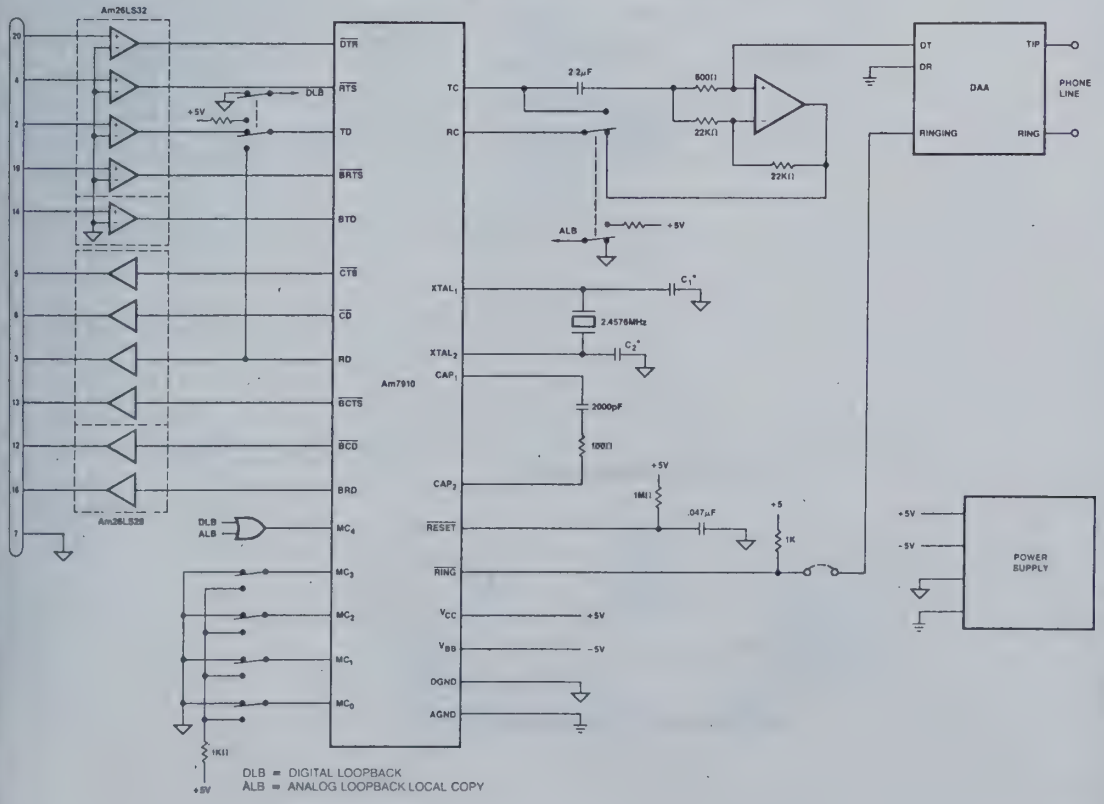

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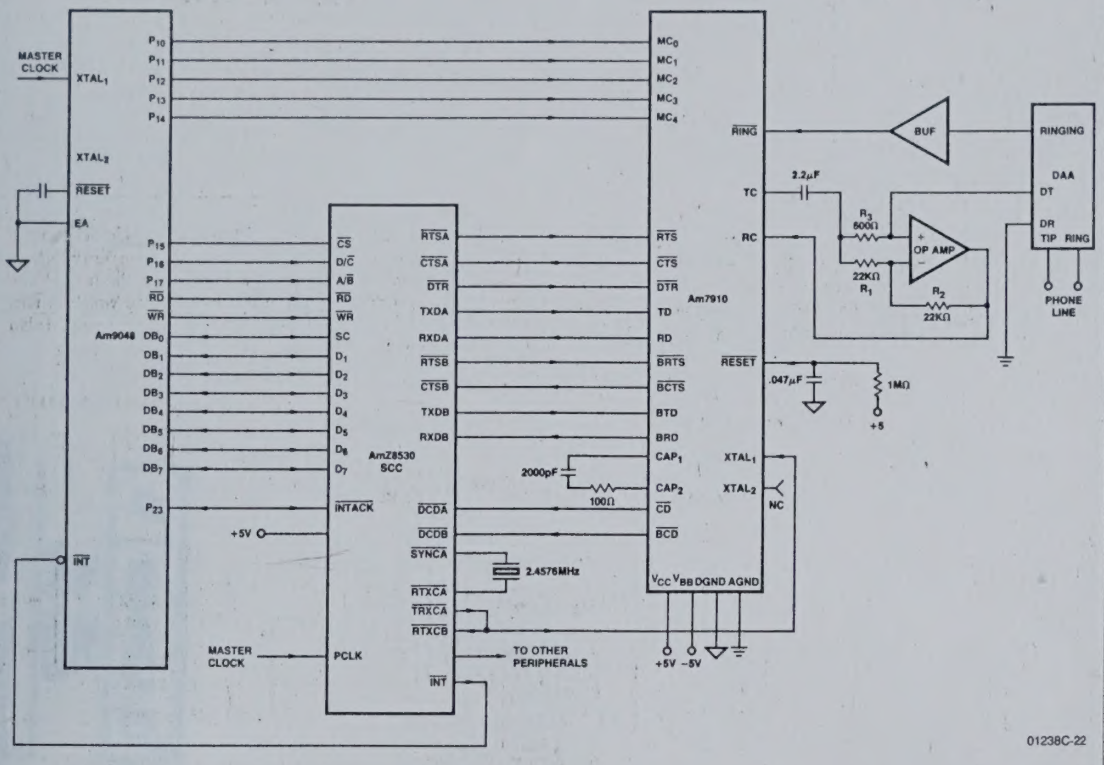
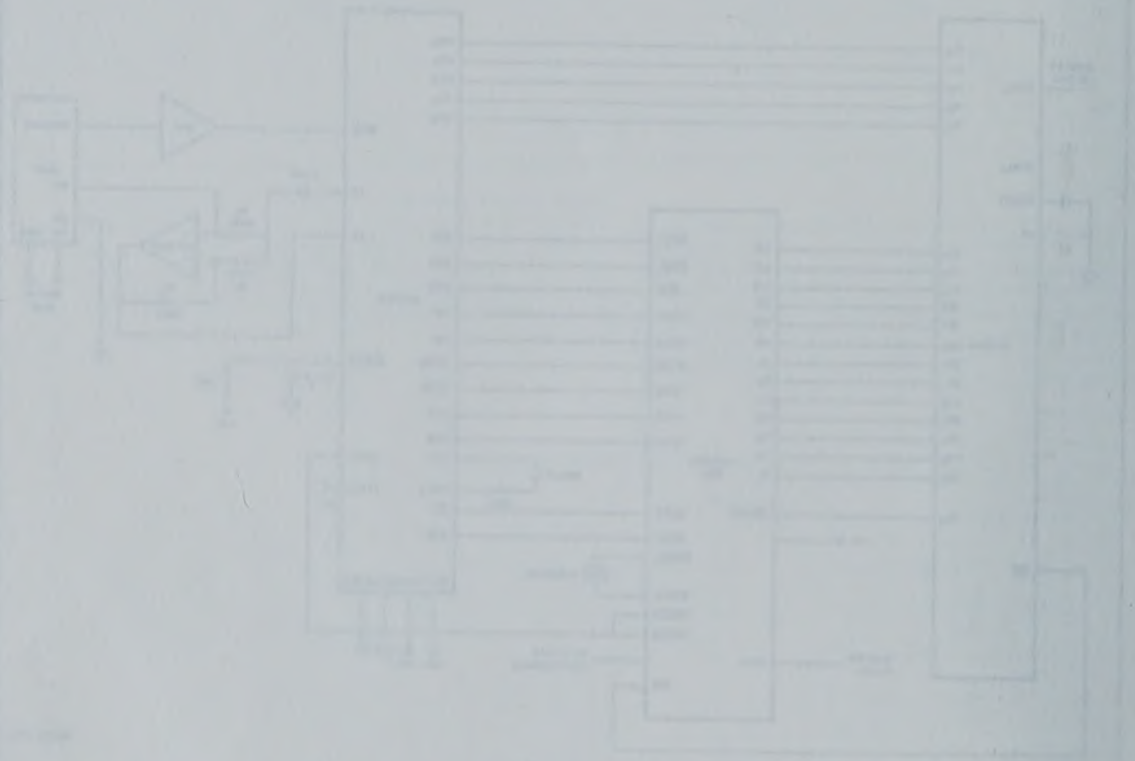
Figure 19. Microprocessor Application



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Cerdip	0° ≤ T_A ≤ +70°C	Am7910DC
Plastic DIP		Am7910PC
Leadless Carrier		Am7910LC

Plastic and leadless carrier packages to be announced.



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